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Review of sub-electron noise CMOS image sensors

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ABSTRACT: Low-light imaging applications, like astronomy or microscopy, require low-noise image sensors with a noise level far below $1\text{ e}^-_{\text{RMS}}$. As such, single-photon detection can be achieved, which is the pinnacle of image sensing. Existing imaging technologies capable of detecting and resolving individual photons, like Photomultiplier Tubes (PMT), Single Photon Avalanche Diodes (SPAD), and Electron Multiplication Charge-Coupled Devices (EMCCD), employ internal multiplication of the primary electron. Although these have noise far below $1\text{ e}^-_{\text{RMS}}$, these methods suffer from two performance-limiting properties: dark counts and excess noise.

This paper surveys solutions for photo charge integrating active pixel sensors (APS) and classic CMOS image sensor (CIS) technology. For integrating image sensor pixels, the readout noise at the pixel frontend must be substantially less than $0.3\text{ e}^-_{\text{RMS}}$ to enable quantum-limited photon detection. APS pixels separate the photo charge sensing and the charge-to-voltage conversion node. This results in a high in-pixel conversion gain and the cancellation of the kTC noise with correlated double sampling (CDS). The pinned photodiode in APS has benefits regarding dark current and rivals the charge-coupled devices (CCD) performance. Continuous improvement of CIS over the last two decades has led to the ubiquitous replacement of CCD by CIS. In this survey, we review the publications that report a noise figure close to $0.3\text{ e}^-_{\text{RMS}}$ or lower and explore the device and circuit techniques used and breakthroughs reached.

KEYWORDS: Analogue electronic circuits; Front-end electronics for detector readout; Photon detectors for UV, visible and IR photons (solid-state); VLSI circuits

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1 Introduction

CMOS (Complementary Metal-Oxide-Semiconductor) image sensors have revolutionized numerous applications in imaging technology, ranging from consumer electronics to scientific exploration. A critical aspect of their performance is their ability to capture high-accuracy images under extreme conditions, such as low-light environments. Achieving ultra-low noise in CMOS sensors is paramount for astronomy, biomedical, life science imaging, and quantum imaging applications. This paper reviews advancements in ultra-low-noise CMOS image sensors, focusing on noise mechanisms, innovative pixel designs, and associated tradeoffs.

2 Background

2.1 Historical development

The evolution of imaging technologies has seen a significant paradigm shift with the widespread adoption of CMOS image sensors. CMOS image sensors initially lagged behind CCDs (Charge-Coupled Devices) despite being introduced in the 1960s before CCDs. Full analog CCDs excelled in imaging applications thanks to their superior dynamic range, smaller pixel sizes, lower fixed-pattern noise (FPN), and better sensitivity than their CMOS counterparts [2]. CCDs optimized for scientific use achieve sub-electron noise through non-destructive readout, but at low frame rates, limiting their application outside astronomy [4]. They had a maximum conversion gain of $20 \mu\text{V}/e^-$, along with issues like poor power efficiency, blooming, smearing, and lack of integration with analog and digital circuits. These drawbacks led to the resurgence of CMOS image sensors in the early 1990s [3, 5]. By the early 2000s, CMOS APS gained popularity. It still had limitations in dynamic range and sensitivity compared to CCDs, which limited its use in scientific fields. Sustained improvements and breakthroughs made CIS surpass CCD by combining high frame rates, reasonable pixel sizes, and equivalent Quantum Efficiency (QE) with notably lower noise levels [2].

2.2 Photon-counting CMOS image sensors

The accurate detection of faint celestial objects, faint scattered signals in Raman spectroscopy, the reliable representation of light-sensitive micro-organisms in fluorescence microscopy, or precise photon estimation in quantum imaging depends heavily on the sensor’s readout noise. In such applications, individual photon detection is essential [1]. Historically, CIS and CCD struggled with low-noise readout. To address this, researchers developed detectors like PMTs, APDs, EMCCDs, SPADs, etc., that amplify the primary photo-generated electrons by a factor of a few hundred to millions. At the electron level before readout, this amplification reduces noise to far below $1\text{ e}^-_{\text{RMS}}$, providing single photon detection [1]. However, the inherent drawbacks of such detectors limit their use for the applications mentioned previously. On the other hand, improvement in noise, speed, and quantum efficiency at lower cost in CMOS image sensors has increased their use in such quantum-limited photon detection applications. Photoelectron counting in CIS with 90% accuracy needs input referred noise of $0.3\text{ e}^-_{\text{RMS}}$, whereas single photon detection needs $0.39\text{ e}^-_{\text{RMS}}$ [6].

3 Advancements in ultra-low-noise CMOS image sensors

As shown in figure 1, a four-transistor pixel with a pinned photodiode (PPD) is commonly used in imaging applications for its low readout noise [3]. Achieving sub-electron noise levels is complex due to interdependent design parameters. Key optimizations include lowering dark current in the PPD, reducing floating diffusion (FD) node capacitance for higher conversion gain, and employing low-noise, high-gain pixel transistors. Techniques like CDS and correlated multiple sampling (CMS) also help reduce column readout circuit noise. The device optimization and noise reduction techniques are discussed in this section.

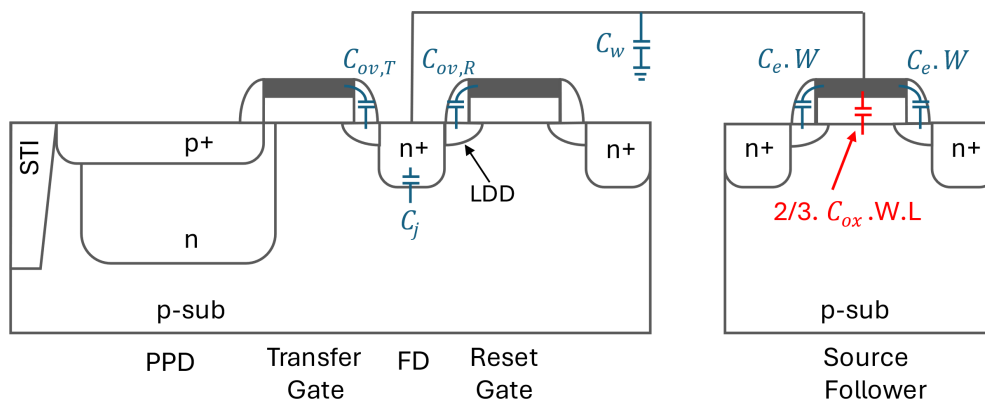


Figure 1. Cross-section of a conventional 4T pixel showing the contribution of different parasitic elements to C_{FD} capacitance. Recreated from [19].

3.1 Lowering C_{FD} for higher conversion gain

In PPD, the collected electrons are transferred to the FD node to get a voltage signal inversely proportional to C_{FD} . It's a contribution of the overlap of FD with gates of reset ($C_{ov,R}$) and transfer ($C_{ov,T}$) switches, p-n junction capacitance between FD and p-epi in contact (C_j), the parasitic capacitance of SF (Source Follower) NMOS, and metal routing capacitance (C_w). Previous studies [7, 8]

have demonstrated the reduction of C_{FD} by implementing various process-level techniques. Notable techniques include the omission of the lightly doped drain (LDD), the reduction of the dopant dose for the n+ implant in the FD node, and the removal of the p+ channel stop implant situated beneath the FD implant, thereby reaching a C_{FD} of 0.66 fF [8]. A research group from Dartmouth University introduced a pixel architecture called “Jot,” claiming single-photon detection. Pushing the FD capacitance to the bare minimum, a noise level of $0.29 e_{RMS}^-$ with CDS and $0.19 e_{RMS}^-$ with 8-fold CMS was reported [9]. The drawback of the architecture is a full well of 200 electrons. A reset-gate-less CIS with a $0.27 e_{RMS}^-$ noise was published in 2015 [10]. The key contribution, C_{FD} of 0.72 fF, needed a maximal reduction of the coupling capacitance of the FD node to the transfer gate (TG) and reset gate. Unlike conventional pixels, the FD node is reset with the punch-through mechanism by applying a high voltage (25 V) at the reset-generating implant close to the FD node. The same issue was addressed using an adjustable-gain 5T pixel architecture in 2020 [11]. In this pixel, the reset was implemented by an intermediate implant between the PPD and the FD node in a 180 nm CIS process. Without any process refinement, the pixel with C_{FD} as low as 0.64 fF achieved a noise of $0.32 e_{RMS}^-$.

3.2 Flicker noise reduction

As all other noise sources can be arbitrarily reduced or canceled, the $1/f$ noise of the pixel source follower (SF) typically limits the noise performance. Early efforts to minimize $1/f$ noise have used buried channel MOSFETs as SF. Here, the charge carriers flow at a distance from the Si-SiO₂ interface [12–14]. The design in [11] utilized the lower K_F of PMOS and thin gate oxide to reach the sub-electron noise figure. A different approach for reducing flicker noise contribution was published [15], involving inversion-accumulation cycling of in-pixel PMOS as a common source amplifier. Cycling a MOSFET between inversion and accumulation regions erases the memory associated with traps, which makes consecutive samples uncorrelated. A noise of $0.34 e_{RMS}^-$ was attained with 1600 samples after cooling the sensor to -40 °C. Another approach is the multi-gate SF-based pixel architecture published in 2022 [16], demonstrating a simultaneous increase in conversion gain and reduction in $1/f$ noise.

3.3 Low-noise column readout circuit techniques

Amplification of the signal close to its source is a straightforward way to reduce input-referred noise in further stages. The work in [17] utilizes a PMOS inside the pixel as a common-source amplifier with a load resistor in the column to achieve a noise of $0.86 e_{RMS}^-$ with good linearity. [18] reports a $0.5 e_{RMS}^-$ noise CIS with in-pixel NMOS of row pixels used as a configurable differential amplifier input pair. A PGA (Programmable Gain Amplifier) and CDS are generally observed in low-noise CIS for better noise and FPN reduction [19]. CMS is popular in several ultra-low noise CIS as it reduces noise beyond simple CDS [9–11]. With an increase in the number of samples in CMS, the thermal noise is reduced by a factor of $\sqrt{M}$, unlike flicker noise, which cannot be reduced beyond a specific limit [19].

3.4 Non-destructive readout

NDR (Non-Destructive Readout) was demonstrated in the 1990s in CCDs. It overcame the $1/f$ noise problem and reached sub-electron noise in CCDs with a “skipper” mechanism using a “floating gate” amplifier [4]. It allows measurement of integrated charge multiple times non-destructively. The average of M samples reduces the readout noise by a factor of $\sqrt{M}$. A new take on this concept was published recently [20, 21]. [20] explains the theoretical analysis and simulation results of

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