

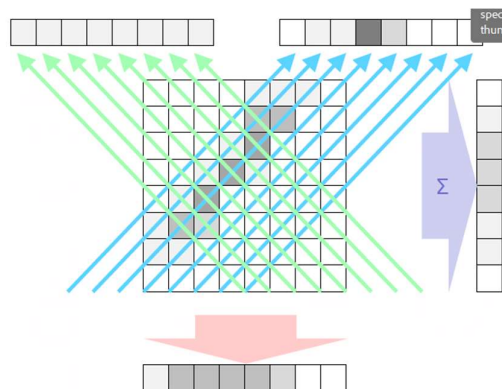
Proposal for Master Thesis

Fixed ratio image compression

The eternal most important limiting factor in high-speed image sensors is to get the data off chip. Today's fastest image sensors have aggregate output rates of 10 to 100 Giga pixel per second. E.g. a 2000 x 2000 pixel imager, running at 10000 frames per second produces 40 billion pixel values per second. When 10-bit AD is converted, one spits 400 billion bits per second, equivalent to 1 (one) Ultra HD Blu-ray per second, or about a hundred (100) CD-ROMs per second. Assuming 10 gigabit/second output stages (as with JESD204B), one needs 40 such stages running in parallel. Although this is feasible, it is hard to stay in specs for system complexity and power dissipation.

One path to significantly reducing the interconnect complexity and the total power dissipation is to compress the image information at the source, i.e. on-chip, just before or just after the ADC conversion.

As the frame rate, or pixel rate is constant, and as the data channel as well has a constant rate, such compression must have a fixed compression ratio. Established compression algorithms as used in JPEG and MP4 *do not have* that property.



In this master thesis we will reckon the options. There are many aspects to this development that can be selected by the student depending on their skills and interests:

- Image sensor IC design, electro-optical design and design verification
- Mathematical approach and high-level concepts
- Literature study
- Building a hardware system, consisting of FPGA, packaging, interfacing to computer systems or camera systems
- Software verification of algorithms

The thesis work includes a prior internship; the total duration of the thesis is more than 6 months.

Student background can be diverse: engineering, physics, mathematics, ICT faculties. Problem solving talent is required.

Please send your application letter and CV to jobs@caeleste.be.