Caeleste BV
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Proposal for Master Thesis

8B10B or JESD204 on FPGA and on an image sensor

JESD204 is a family of protocols that enables CML (LVDS) wire pairs to run data rates of multiple gigabits per second (Gbps).

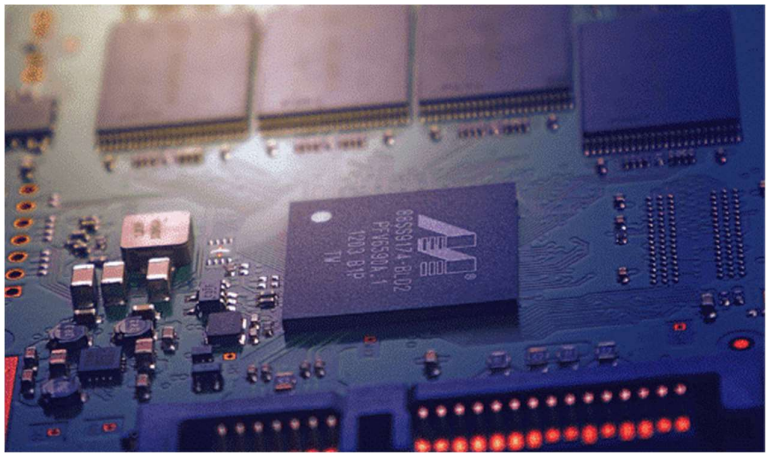
The secret behind is simple. A CML wire pair can deliver approximately 1Gbps of raw data before significant bit errors occur. These errors are due to imperfections in interconnections, imperfect terminations, dispersion, faulty synchronization, drift etc.

The JESD204's 8B10B protocol essentially encodes raw data bytes (8-bit) as 10-bit words. While the number of bits to be transmitted increases, the protocol bears essential advantages:

- The 10-bit word is bit-balanced: its has, on short time average, an equal number of 0's and 1's.
- This essentially removes the DC component from the signal, and narrows the spectral content of the signal around half the bit rate. This drastically reduces dispersion as main source of bit errors.
- It guarantees bit transitions at least once per 5 bits. This facilitates recovery of the clock from the data stream itself. The transmission becomes insensitive to microphony, temperature variations and slow jitter.

The objectives of this thesis project are to:

- Describe and simulate the 8B10B encoding in VHDL or Verilog,
- Synthesize the code to FPGA, and verify,
- Ultimately, retarget the code to CMOS, as compatible with CMOS image sensors.



Student background: digital electronics, embedded systems. Relevant knowledge of VHDL or Verilog.

Please send your application letter and CV to jobs@caeleste.be.