# Charge domain binning using potential differences between photodiodes

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## ABSTRACT

We show a CMOS image sensor combining charge domain global shutter (GS), true high dynamic range (HDR), back side illumination (BSI) with back bias, radhard designed. The design is stitched and might reach resolutions with a multiple of 1k*1k pixels up to wafer scale. Pixel pitch is 15 µm. The device is processed on a high resistive, 22 µm thick BSI wafer in LF11IS technology.

We describe the sensor's experimental method for *charge domain* binning.

Historically charge domain binning has been realized successfully in CDDs, were proper clocking of CCD electrodes merges charges of neighboring pixels into one charge packet. The readout of that charge package happens with the read noise of a single "normal", "un-binned", pixel. Charge domain binning thus realizes an increase of SNR with a factor equal to the amount of pixels in the "bin".
In CMOS pixels, charge domain binning by CCD transfers is not possible. One has demonstrated charge domain binning in so-called shared pixels, with some limitations.

This novel charge domain binning concept is illustrated in Figure 1. One pixel per group of two by two is enabled for charge collection whereas the others are programmed to not, or to a lesser extent, collect charges. This is realized by keeping the non-collecting photodiodes floating or explicitly biased at a lower potential. The pixels that are intended to collect "C" have higher potential. Under such bias conditions, in high resistive material, the electric field lines extend laterally under the non-collecting pixels.

In Figure 3, the principle is clarified in 1 dimension. The two outer pixels are operated to be actively charge collecting, the middle pixel is operated to be not collecting. The photodiode is made floating by permanently turning off the transfer gate TG. As the photodiode has no path to drain the photocurrent, its potential will drop to the limit that the PPD-substrate diode becomes forwards biased, or that the TG leaks.

**Performance and optimization**
Ideally or theoretically, the configuration described should result in a factor 4 photoresponse increase. First measurements however show only a factor of 1.4 improvement in photoresponse when charge binning is applied. The effect is symmetric in X and Y.
In [1] a hypothesis was put forward: Due to the low depletion voltage of the pinned photodiodes of this particular device (0.1V), there is almost no bending of the electric field from the bulk towards the charge collecting diodes. Using TCAD simulation, we will show how the operation can be improved.

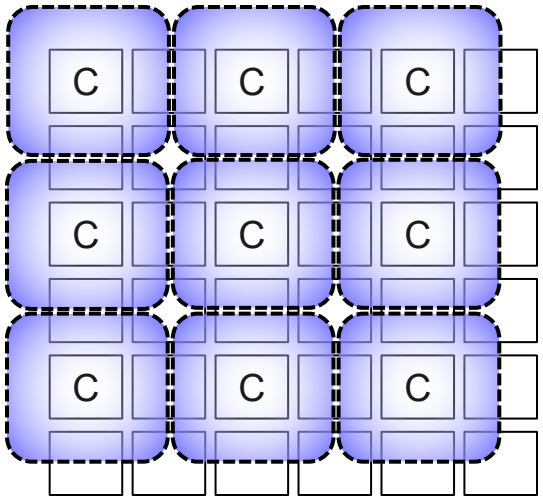


*Figure 1:Concept of a 2x2 kernel implementation of charge collecting ("C") and non-collecting pixels*

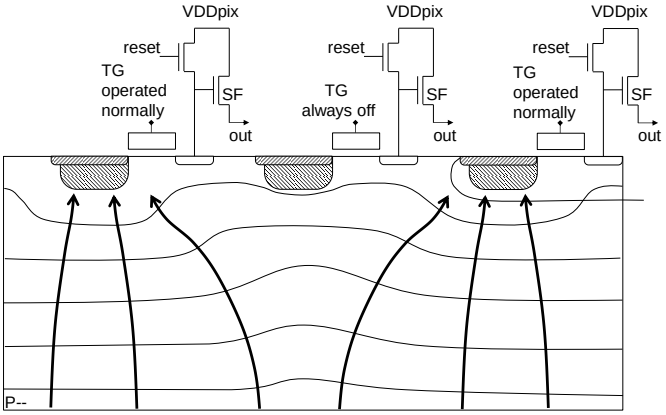


*Figure 3: Cross-sections of 3 pixels showing the charge domain binning concept*

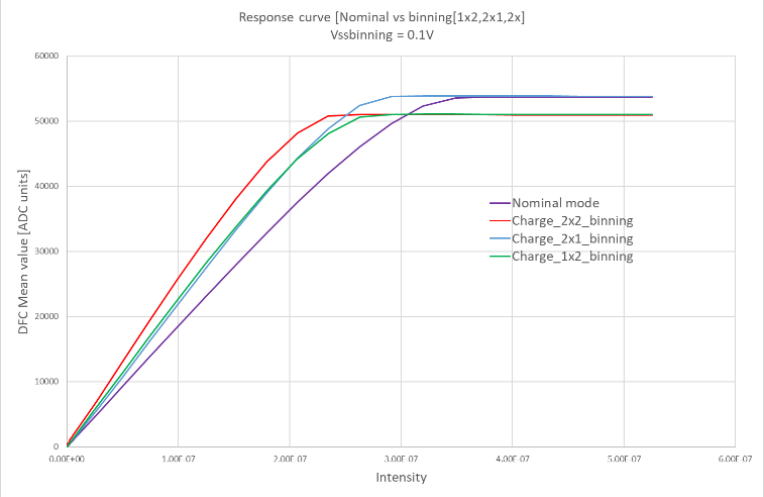


*Figure 2: measured photoresponse for nominal mode, charge binning 2x2, 2x1 and1x2*

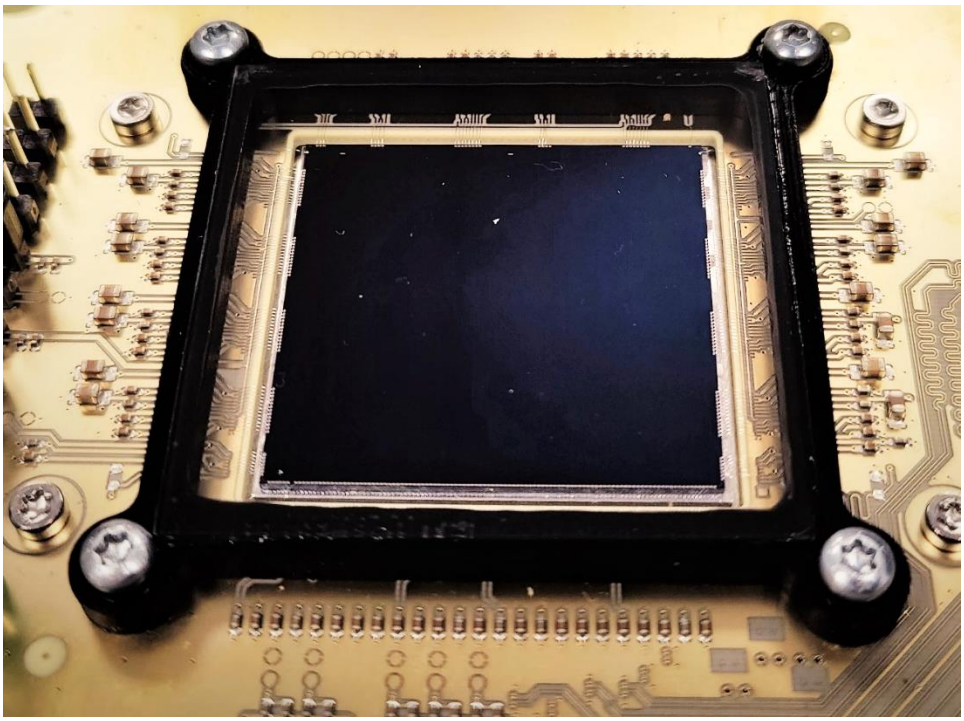

*Figure 3 picture of 2k x2k image sensor*

References


1. A. Kalgi & al., "High dynamic range CIS with true global shutter and charge domain binning", ESA image sensor workshop, Noordwijk, 22 Dec 2022