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FLAMES

High-Speed Flash-LiDAR CMOS Imager for Landing Missions

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Outline



- Who we are
- Motivation
- Pixel concept
- Architecture of the sensor
- Simulation results
- Conclusions & Outlook



WHO WE ARE

22/06/2023

Caeleste's mission





Be the supplier of beyond state-of-the-art custom-designed **CMOS** image sensors

22/06/2023

Who we are

Address:

- Hendrik Consciencestraat 1b, 2800 Mechelen, Belgium
- Staff:
 - ~ 40 people





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Vilvoorde

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Machelen

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Business focus





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MOTIVATION

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Motivation

- LiDAR for space applications:
 - Controlled soft landing
 - Navigation of rovers
 - Rendezvous of spacecrafts
- Flash vs Scanning LiDAR:
 - Flash LiDAR Can be smaller and lighter
 - Significant higher measurement rate than scanning LiDAR
 - No moving parts for Flash LiDAR





PIXEL CONCEPT

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Pixel concept

Collecting photodiode:

- centered
- collect photoelectrons

Non-collecting photodiodes:

- 4 corners
- modulate the sensitivity of collecting photodiode

Transistors:





RM1: time gating with RST, no CDS

- Returning laser pulse crossing the falling edge of RST
- Signal can be sampled on C1 only or C1&C2
- No CDS (Correlated Doubling Sampling)



RM2: time gating with SH, CDS

- Returning laser pulse crossing the edges of SH pulses
- Slower time gating due to limited S&H speed
- CDS used for low noise
 - RESET level on C1
 - SIGNAL level on C2



RM3: time gating with PD modulation, CDS

- Returning laser pulse crossing the edges of PD modulation pulse
- Faster time gating than RM2
- CDS used for low noise
 - RESET level on C1
 - SIGNAL level on C2





ARCHITECTURE OF THE SENSOR

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Architecture of FLAMES sensor

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- BSI (Backside illumination) is used
- Pixel array are driven from West & East sides
- Top half and bottom half of the array can be driven separately
- Readout are from North & South sides
 - Each side has 8 LVDS channels
 - Each readout channel has 8 timeinterleaved SAR ADCs
- SPI, Voltage references, etc. are at the four corners



Independent control for top & bottom halves caelest

- 4 signals determine the integration time of the pixel
 - RST, SH1, SH2 & PD
- 2 pairs of LVDS receivers for each signal
- Example: RST
 - LVDS pair: RST<1>, nRST<1>
 - LVDS pair: RST<2>, nRST<2>
- Each LVDS pair can control one half independently or the entire array simultaneously



Scan the pixel array in Y direction

- Y address decoder determine the start position of Y scanning
- Y scanner can scan the array from top to bottom
- Always address 2 rows of pixels at the same time
 - One row is readout at the North
 - Another row is readout at the South
- 500fps @ full frame, up to 2000fps with smaller ROI



Pixel readout chain (1)

Column load:

provide current bias for SF2

Column readout circuits:

- PGA: provide column gain which can be x1, x2, x4 or x8
- S&H stage: Odd & Even capacitor banks for pipelining readout
- Video buffer: to multiplexing pixel signals to ADCs



Pixel readout chain (2)

• X scanner:

- control video buffers
- Clock rate: 43MHz

12-bit SAR ADC:

- 8 readout channels at both North and South sides of the array
- Each readout channel has an 8-way time-interleaved SAR ADC

LVDS driver: х address decoder column<11> column<10> Data rate: 516Mbps column<9> column<8> column<7> column<6: column<5> (column<4> Pixel column<3> column<2> column<1; DATA<7> column<0> CH<6> S&H stage nDATA<7> CH<5> CH<4> CR_odd CH<3> SHR_even CH<2> CR_even Video CH<1> Column PGA VREE 11 LIC Gain = x1, x2, x4, x8 CH<0>DATA<0: ill 12bit IDEO S CS_odd Serializer x8 Interleave SHS_even nDATA<0> SPI Column readout circuits (VIDEO R VIDEO S)



SIMULATION RESULTS

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RM1 time gating sharpness

- Laser pulse length is 2ns
- Sweep laser pulse delay:
 - from -5ns to +5ns around the falling edge of RST
- Time gating sharpness is ~2ns when fall time of RST < 4ns</p>



RM2 time gating sharpness (1)

- Laser pulse length is 2ns
- Sweep laser pulse delay:
 - from -5ns before SH1 pulse to +5ns after SH2 pulse
- Minor signal degradation when SH pulse length > 10ns



RM2 time gating sharpness (2)

- Laser pulse length is 2ns
- Sweep laser pulse delay:
 - from -5ns before SH1 pulse to +5ns after SH2 pulse
- Minor time gating sharpness improvement when rise/fall time of SH <4ns



RM3 time gating sharpness

- Laser pulse length is 2ns
- Sweep laser pulse delay:
 - from -5ns before SH1 pulse to +5ns after SH2 pulse
 - Time gating sharpness is ~2ns when fall time of PD < 2ns



TCAD: photodiode sensitivity modulation

Simulation conditions:

- Fully depleted 10µm epi thickness
- OFF state: Non-collecting diodes biased at 5V
- ON state: Non-collecting diodes biased at 0V

Learned from TCAD results:

- Fully-depleted high-res epi is required
- No P-Well between collecting diode & noncollecting diodes
- PSUB connection is required between collecting diode & non-collecting diodes to block large surface leakage
- ON-OFF photocurrent ratio is between 2 and 5 depending on the sizes of the diodes

5V







CONCLUSIONS & OUTLOOK

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Conclusions:

- 1.3Mpix, 500fps Flash-LiDAR CMOS image sensor is designed
- Pixel can operate in 3 different modes with their own pros and cons
- Time gating sharpness can be better than 5ns in RM1 & RM3, and better than 10ns in RM2
- Readout noise is expected to be below 10e- with CDS

Outlook:

Tape out will be around the beginning of next month





For more information or questions, please contact:

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Scan the QR-code to visit our website: www.caeleste.be

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