# FLAMES – High-Speed Flash-LiDAR CMOS Imager for Landing Missions

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***Abstract*— A high-speed Flash-LiDAR CMOS image sensor which is named FLAMES for landing missions is presented. The sensor features 1280(H) x 1024(V) array size with a pixel pitch of 14µm. It offers a full-frame capture rate of 500fps, up to 2000fps for smaller ROI, such as 500(H) x 500(V). The sensor can operate in 3 different modes, and its time gating sharpness is anticipated to be faster than 5ns. When correlated double sampling (CDS) is utilized, the readout noise is expected to be less than 10e-. This paper discusses the architecture of FLAMES sensor, the design considerations employed to achieve high speed and fast time gating and presents relevant simulation results.**

***Keywords*— *flash lidar, high speed, CMOS imager, BSI***

## I. Introduction

LiDAR technology is recognized as a key enabling technology for future autonomous landing missions and space operations involving the rendezvous between two spacecraft in orbit. Traditional LiDAR systems utilize scanning mechanisms and complex receiving systems, limiting their speed and efficiency. To overcome these challenges, high-speed Flash-LiDAR CMOS imagers have revolutionized the field by providing real-time, high-resolution 3D imaging capabilities. These advancements enable accurate and precise terrain mapping, unexpected obstacle detection, and collision avoidance, ensuring safe landings. In this paper, we provide an in-depth analysis of technical challenges and on-going research effort associated with FLAMES, a high-speed BSI CMOS image sensor designed for landing missions.

## II. Flash-LiDAR System of FLAMES

The architecture of the Flash-LiDAR system utilized in FLAMES is shown in Fig. 1. In this system, a laser pulse with a pulse length of a few nanoseconds or less is emitted towards the target objects and gets reflected to the detector.

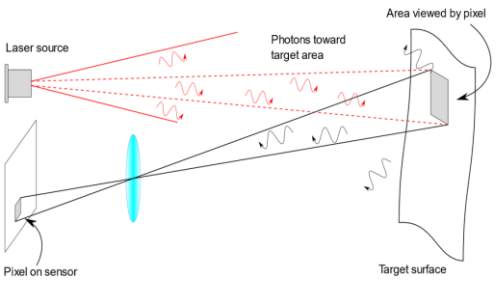


Fig. 1 Architecture of Flash-LiDAR system of FLAMES

When the returned laser falls into the short time gating period as shown in Fig. 2, the signal experiences an increase. By programming the time gating delay, it is possible to detect the rising edge of the signal. This enables the estimation of the time lapse (Δt) between the emitted laser pulse and the returned laser pulse. The distance (d) between the detector and the target object can be calculated by using the following formula:

$$d = \frac{\Delta t}{2} c \quad (1)$$

where c is the speed of light. In addition, shorter (or sharper) time gating period can enhance the definition of the rising edge of the signal, resulting in better distance estimation.

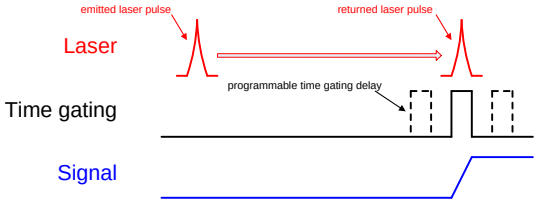


Fig. 2 Time gating for distance estimation

By combining multiple images, for example 20 images with different time gating delays, it is possible to construct the 3D information of the full frame.

## III. Pixel Concept

### A. Principles of Operation

The circuit diagram of the pixel is shown in Fig. 3, and the corresponding layout is shown in Fig. 4. The pixel pitch is 14µm.

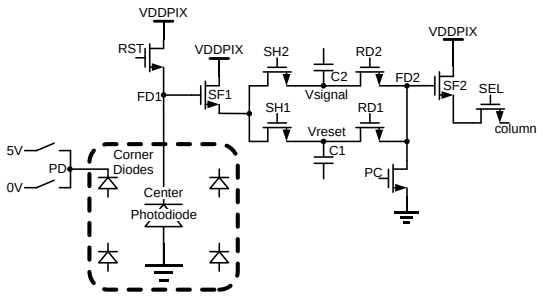


Fig. 3 Circuit diagram of the pixel

Within each pixel, the collecting photodiode (depicted as blue octagons in Fig. 4) locates at the center of the pixel and is responsible for capturing photoelectrons. Its sensitivity can be modulated by biasing the non-collecting photodiodes at the four corners of the pixel (depicted as red octagons in Fig. 4). These corner photodiodes can be biased either at a high level (typically 5V) or a low level (typically 0V) through PD signal. To initiate the integration, a reset transistor known as

RST is utilized to reset the collecting photodiode. In addition, a PC pulse is applied to pre-charge FD2, both C1 and C2 capacitors to ground level while both RD1 and RD2 are on. Following the photo integration period, the signal present on the FD1 node, associated with the collecting photodiode, can be sampled on either capacitor C1 or capacitor C2 by activating SH1 or SH2. By turning on either RD1 or RD2, the signals Vreset or Vsignal become accessible on FD2, which can be read out via SF2 by enabling the SEL transistor. To eliminate potential memory effect, PC transistor is employed to pre-charge FD2 to ground level prior to the arrival of each new signal.

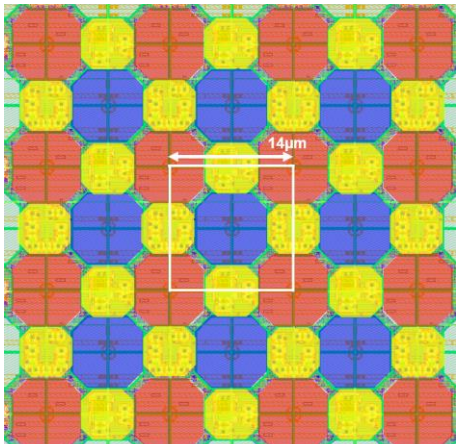


Fig. 4 Layout of the pixel

## B. *Pixel Readout Modes*

The pixel has 3 different readout modes: RM1, RM2 & RM3. Their operational principles are described as follows:

### *1) RM1 mode*

In RM1 mode, the falling edge of the RST signal is utilized for time gating. The timing diagram, illustrating the control signals for the pixel is given in Fig. 5.

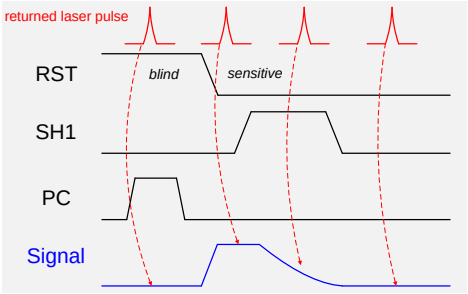


Fig. 5 Timing diagram of pixel control signals for RM1

As illustrated in Fig. 5, if the returned laser pulse arrives prior to the falling edge of RST signal, the signal remains at low level. However, once the returned laser pulse crosses the falling edge of RST signal, the signal increases and reaches its maximum when the returned laser pulse arrives after the falling edge of RST signal. SH1 (or both SH1 and SH2) pulse is given after the falling edge of RST signal to sample the signal on the capacitor C1 (or on both C1 and C2), so in this mode,

$$Signal = Vreset \tag{2}$$

The time gating sharpness of this mode is determined by the falling time of RST signal, which can be made shorter than 2ns. However, one disadvantage of this mode is its relatively high readout noise due to the absence of correlated double sampling (CDS).

### *2) RM2 mode*

In RM2 mode, the time gating is determined by the SH pulse. Fig. 6 shows the timing diagram for this mode, illustrating the control signals and their respective timings.

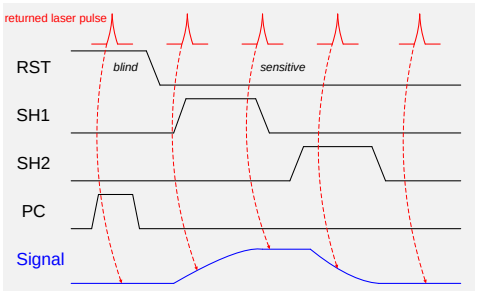


Fig. 6 Timing diagram of pixel control signals for RM2

In this mode, after turning off RST transistor, SH1 pulse is applied. The pixel signal is then sampled on capacitor C1, Subsequently, the SH2 pulse is applied to sample the pixel signal once again, this time on capacitor C2. Consequently, in this mode, the signal can be calculated as the difference between Vreset and Vsignal as expressed in (3) which is called CDS:

$$Signal = Vreset - Vsignal \tag{3}$$

As shown in the figure, before the returned laser pulse arrives at the SH1 pulse, the signal remains at a low level. As the returned laser pulse falls within the duration of the SH1 pulse, the signal gradually increases and reaches its maximum value towards the end of the SH1 pulse. However, if the returned laser pulse is delayed further, the amplitude of the signal gradually decreases. When the returned laser pulse delay is approaching the end of the SH2 pulse, the signal returns to a low level again.

In RM2 mode, the rising edge of the signal is comparatively slower than in RM1 mode due to the limited signal settling time. However, an advantage of RM2 mode is the significantly lower readout noise which is achieved by employing CDS.

### *3) RM3 mode*

In RM3 mode, the sharpness of the time gating is determined by the falling edge of the PD signal. The timing diagram, depicted in Fig. 7, illustrates the control signals used to operate the pixel in this mode.

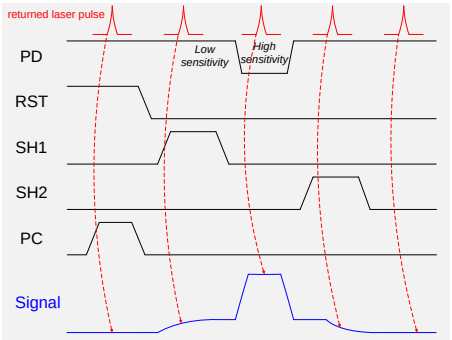


Fig. 7 Timing diagram of pixel control signals for RM3

The difference between RM2 and RM3 modes lies in the behavior of the non-collecting photodiodes, i.e., PD in Fig. 4, located at the four corners of the pixel. In RM2 mode, these

photodiodes are maintained at a low level, typically 0V, throughout the operation. On the other hand, in RM3 mode, these photodiodes are modulated between a high level and a low level during the gap between SH1 and SH2 pulses.

By biasing the corner photodiodes at a high level, the width of their depletion region increases. As a result, a significant portion of the photoelectrons will be drawn towards these non-collecting photodiodes. This effectively reduces the sensitivity of the collecting photodiode located at the center of the pixel. Conversely, when the corner photodiodes are biased at a low level, the width of their depletion region becomes minimal. In this case, most of the photoelectrons will be directed towards the collecting photodiode.

Like RM2, when the returned laser pulse falls within the duration of the SH1 pulse in RM3 mode, the signal increases gradually but its amplitude is much smaller than that in RM2 due to the high-level biasing of the corner photodiodes through PD. When the returned laser pulse coincides with the period when corner photodiodes are biased at a low level, the signal amplitude undergoes a significant increase. If the returned laser pulse is delayed further and reaches the SH2 pulse, the signal amplitude gradually decreases and returns to the lowest level again, mirroring the behavior observed in RM2 mode.

RM3 mode combines the advantage of fast time gating speed, as seen in RM1 mode, and low readout noise by employing CDS like in RM2 mode. The optimal performance of RM3 mode can be obtained by maximizing the sensitivity ratio between the non-collecting photodiodes biased at high and low levels. This can be verified and optimized through TCAD simulations.

## IV. Architecture of The Sensor

### A. Top level architecture

The top-level architecture of the sensor is shown in Fig. 8.

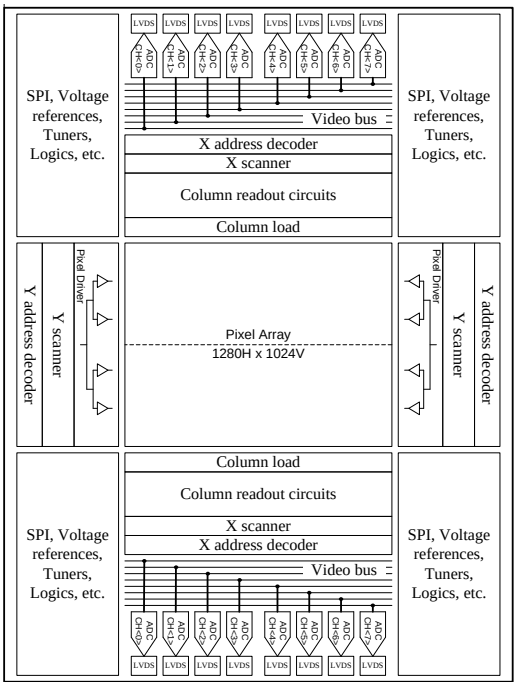


Fig. 8 Top level architecture of the sensor

The sensor features a pixel array with a resolution of 1280(H) x 1024(V), centrally positioned within the sensor. Notably, the top and bottom halves of the array can be independently controlled for time gating, and detailed discussions on this feature can be found in section C. To drive the pixel array, signals are provided from both the West and East sides. The Y periphery includes essential components such as a Y address decoder, responsible for determining the starting point for the region-of-interest (ROI) along the Y direction. In addition, a Y scanner, implemented as a shift register, scans the array from top to bottom, while a pixel driver generates all the necessary control signals for the pixel.

The readout circuits are symmetrically located at the North and South sides of the pixel array. These circuits comprise a column load, a column readout circuitry which includes programmable gain amplifier (PGA), sample and hold (S&H) capacitors and video buffers, an X scanner, and X address decoder, analog-to-digital converters (ADCs), and LVDS drivers. Furthermore, the chip includes other supporting components such as the serial peripheral interface (SPI), voltage references, tuners to control the current bias of amplifiers, and additional logic circuits, strategically positioned at the four corners of the chip.

### B. Pixel readout chain

The addressing and readout process of the pixel array is illustrated in Fig. 9. Every two rows of pixels are addressed and read out simultaneously. One row of pixels is read out from the North side, while another row is read out from the South side. Fig. 10 presents a detailed schematic of the pixel readout chain.

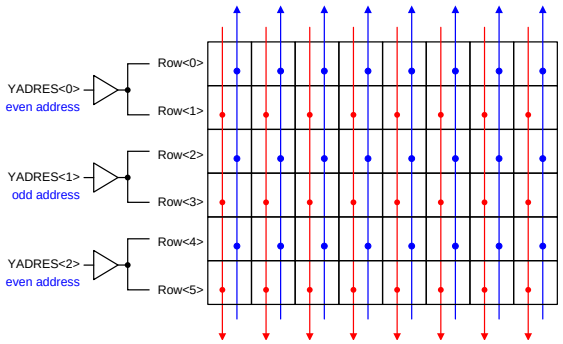


Fig. 9 addressing and readout of the pixel array

In Fig. 10, the schematic shows the key components involved in the pixel readout chain and their interconnections. Here is an overview of the functionality described:

1. The column load provides the current bias for SF2 in the pixel, the column wire is connected to the input of the programmable gain amplifier (PGA).
2. The PGA can be configured with different analog gain options of x1, x2, x4, or x8, depending on the ratio of capacitors Cs and Cf (gain = Cs/Cf).
3. The output of the PGA is then sampled by the sample-and-hold (S&H) capacitor banks. Each capacitor bank consists of two capacitors: CR and CS. The CR capacitor samples either the reset level Vreset from the pixel or an external reference voltage, while the CS capacitor samples the signal level Vsignal from the pixel. Each column has both

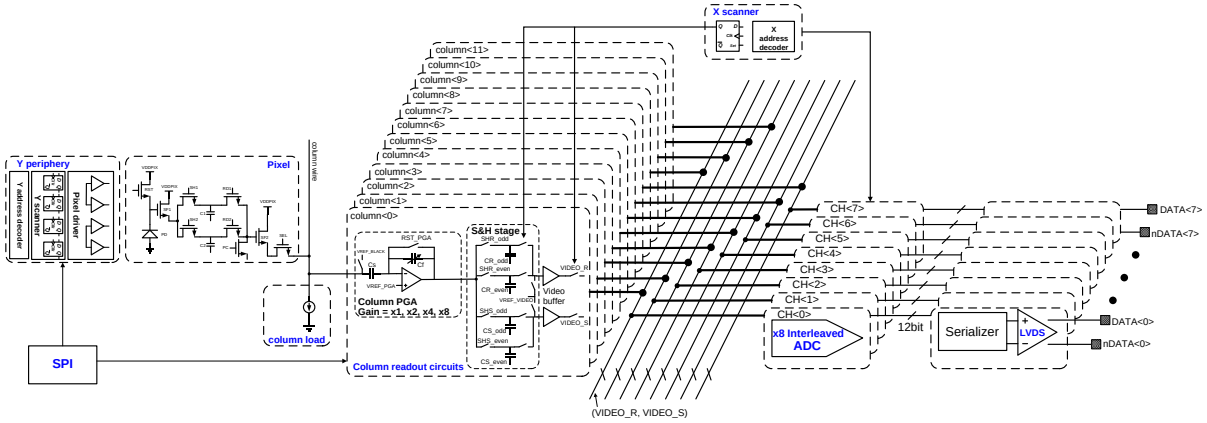


Fig. 10 pixel readout chain

odd and even capacitor banks, which are used for pipelining readout.

4. Pipelining readout is implemented in such a way that while the signals from even-addressed rows of pixels (YADRES<0>, YADRES<2>, etc. in Fig. 9) are being sampled on the S&H capacitors, the signals from odd-addressed rows of pixels (YADRES<1>, YADRES<3>, etc. in Fig. 9) are being read out by the ADCs. This enables continuous and fast readout of pixel signal from the sensor.
5. Each column in the array has two video buffers. One video buffer is responsible for reading out the CR capacitors, while the other video buffer reads out the CS capacitors.
6. X scanner, a shift register, is used to control video buffers to multiplex the pixel signals of all columns onto the video lines (VIDEO_R and VIDEO_S in Fig. 10).
7. The signals present on the video lines will later be sampled and converted by the ADCs. At each side of the chip, specifically the North and South sides, there are eight readout channels, which are labeled DATA<0> to DATA<7>. This corresponds to the presence of eight LVDS drivers. Each LVDS channel is running at 516Mbps and equipped with an 8-way time-interleaved successive-approximation-register (SAR) ADC.

### C. *Independent control for top & bottom halves*

During landing missions, the camera may be tilted towards the landing area's surface. This tilting will result in big differences in the distances between the camera and the surface for the top and bottom halves of the pixel array. To capture 3D information efficiently and rapidly for the entire array, it is desirable to have different time gating delays for the top and bottom halves.

Since the time gating of the pixel is determined by four control signals - RST, SH1, SH2 and PD - it is necessary to independently control these signals for the top and bottom halves of the array. In the case of the RST signal shown in Fig. 11, there are two pairs of LVDS receivers, namely (n)RST<1> and (n)RST<2>, which receive independent input signals. These pairs of receivers are connected to multiplexers that can be configured through SPI registers, namely SEL_RST<1> and SEL_RST<2>. This configuration allows for the independent control of the top and bottom halves of the array, and it is also possible to control the entire array simultaneously via only one pair of input signals.

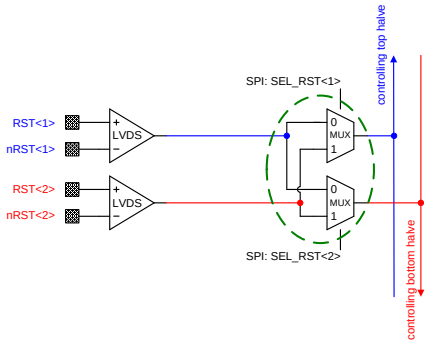


Fig. 11 circuits for independent control for top and bottom halves for RST

The same circuit implementation can be applied to the other three signals. The four signals, RST, SH1, SH2 and PD, are generated and controlled from the four corners of the chip as illustrated in Fig. 12.

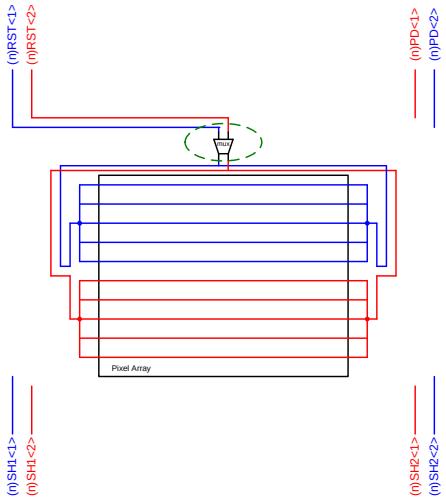


Fig. 12 Implementation for RST, SH1, SH2 and PD signals

## V. TCAD Simulation for Sensitivity Modulation

The functionality and performance of sensitivity modulation in the collecting photodiodes through the alternating bias voltage of the non-collecting photodiodes are evaluated with TCAD simulations.

### A. *TCAD simulation for sensitivity modulation*

TCAD simulation was done in Tower Semiconductor 0.18µm CIS technology with high resistivity 10µm epitaxy. One exemplary simulation result is shown in Fig. 13. By comparing the responses of the collecting photodiodes between the conditions that the non-collecting photodiodes when they are biased at a high level and when they are biased at a low level, the sensitivity ratio can be determined.

Through TCAD simulations, it is possible to gain a better understanding of how to modulate the non-collecting photodiodes to maximize the sensitivity ratio of the collecting photodiode.

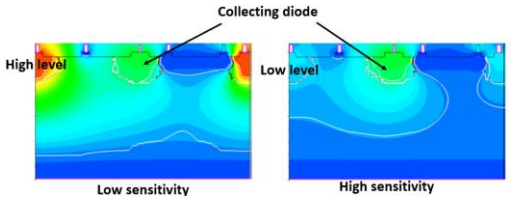


Fig. 13 TCAD simulation setup for sensitivity modulation

From TCAD simulations, we can set the following strategies to obtain the optimal performance:

1. Fully depleted high resistivity epi is required
2. Best sensitivity ratio can be achieved without P-well between the collecting photodiode and the non-collecting photodiodes
3. To ensure radiation hardness and prevent large surface leakage current between the photodiodes, a P-substrate connection surrounding each photodiode is required
4. The sensitivity ratio will be between 2 and 5, depending on the size of the photodiodes. The best pixel design found in TCAD simulation is used as default pixel in the main array. To evaluate the design, variants of pixels with different sizes of the photodiodes are added in the test pixel columns.

## VI. SPICE Simulation for TIMG Gating Sharpness

SPICE simulations are used to evaluate the time gating sharpness of each readout mode. Results and analysis will be presented in the following sections, providing insights into the behavior and characteristics of the sensor. In all the simulations, the laser pulse length is set to 2ns.

### A. *Time gating sharpness in RM1*

The timing diagram of key signals to simulate time gating sharpness in RM1 is shown in Fig. 14. The returned laser delay varies from 5ns before the falling edge of RST to 5ns after the falling edge of RST.

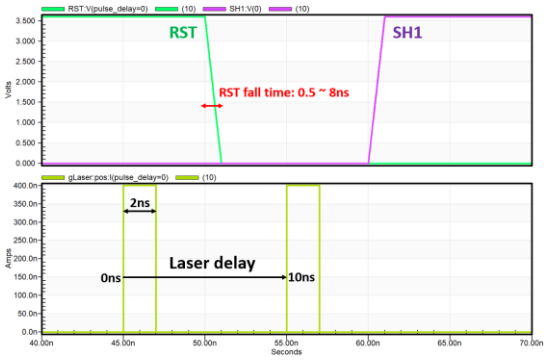


Fig. 14 Timing diagram for time gating sharpness in RM1

The time gating sharpness is simulated with different falling times of RST signal from 0.5ns to 8ns. The result is shown in Fig. 15.

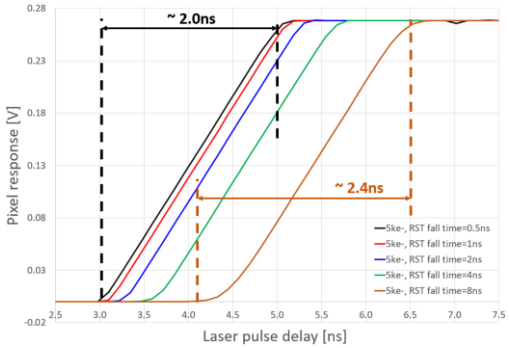


Fig. 15 Time gating sharpness vs RST falling time in RM1

From the simulation result, it is noticed that the best time gating sharpness is 2ns which is limited by the laser pulse length, and there is no performance gain when the falling time of RST signal is comparable with the laser pulse length.

### B. *Time gating sharpness in RM2*

The timing diagram to simulate time gating sharpness in RM2 is shown in Fig. 16. The returned laser delay varies from 5ns before the rising edge of SH1 to 5ns after the falling edge of SH2.

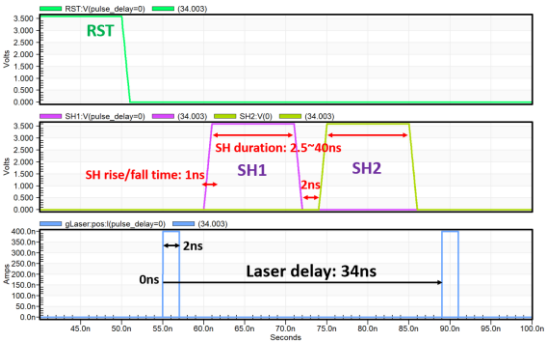


Fig. 16 Timing diagram for time gating sharpness in RM2

The time gating sharpness is simulated with different SH pulse durations from 2.5ns to 40ns. The pulse durations of SH1 and SH2 pulses are set to be the same. The result is shown in Fig. 17.

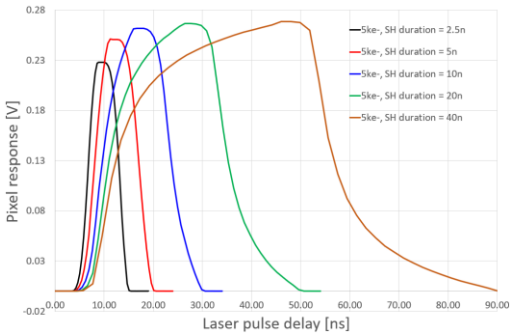


Fig. 17 Time gating sharpness vs SH pulse duration in RM2

The amplitude of the signal degrades when the SH pulse duration is shorter. The degradation is negligible when SH pulse duration is longer than 10ns.

The time gating sharpness with different rising and falling times of SH signal is also simulated. The rising time and falling time are set to be the same and they vary from 0.5ns to 8ns when SH pulse duration is 10ns. The result is shown in Fig. 18. From the results, it is concluded that the time gating sharpness degradation is marginal when the rising and falling times of SH signal can be less than 4ns.

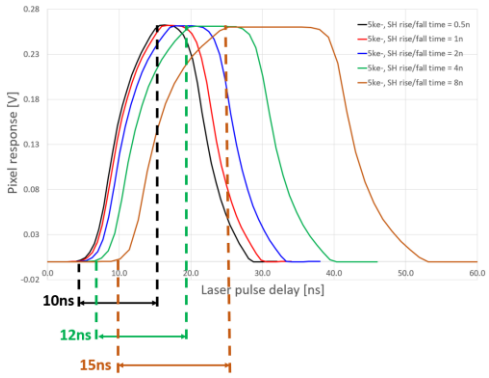


Fig. 18 Time gating sharpness vs rising & falling time of SH signal in RM2

### C. *Time gating sharpness in RM3*

The timing diagram to simulate time gating sharpness in RM3 is shown in Fig. 19. Like the simulations done for RM2, the returned laser delay also varies from 5ns before the rising edge of SH1 to 5ns after the falling edge of SH2. The difference is that PD bias modulation is inserted between the SH1 pulse and the SH2 pulse.

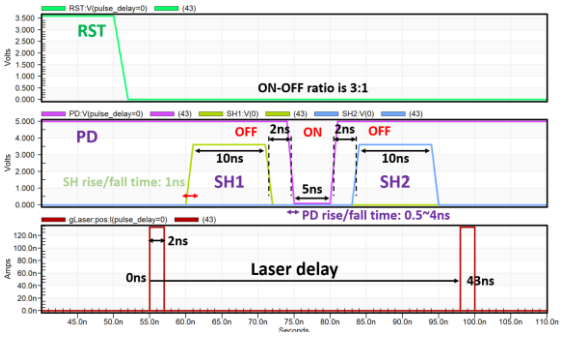


Fig. 19 Timing diagram for time gating sharpness in RM3

The time gating sharpness with different rising and falling times of PD signal is also simulated. The rising and falling time are set to be the same and they vary from 0.5ns to 4ns, and SH pulse duration is 10ns. The result is shown in Fig. 20. Like RM1, there is no performance gain when the rising/falling time of PD signal is comparable with the laser pulse length.

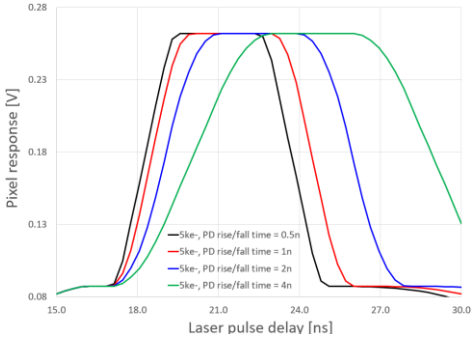


Fig. 20 Time gating sharpness vs rising/falling time of PD signal in RM3

## VII. Conclusions and Outlook

A 1.3Mpix flash-LiDAR CMOS BSI image sensor is designed. The pixel can operate in three different modes-RM1, RM2, and RM3-with their own pros and cons. Time gating sharpness can be better than 5ns in RM1 and RM3, and better than 10ns in RM2. Readout noise is expected to be below 10e- with CDS.

The tape out of the sensor is expected to happen in July 2023.

## Acknowledgment

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