Space and scientific CMOS
image sensors workshop
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High dynamic range CIS with true global shutter and charge domain binning

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ESA contract 4000116089 “European Low Flux Image Sensor”

Purpose

The “ELFIS2” image sensor features the combination of

1. BSI (Backside illumination)
   → High QE also at near infrared wavelength
2. TID and SEL/SEU radiation-hard design
3. “True”, Motion Artifact Free (MAF) **HDR** (High Dynamic Range)
   ⇒By reading the same photocharge on two different conversion capacitances
   ⇒All values over the full dynamic range have identical integration time and are synchronous
4. IWR Global shutter using “**GS**” CMOS technology, which
   ⇒ Allows low noise readout using CDS (correlated double sampling)
   ⇒ Enabling Global Shutter without dark current penalty

Nice to have

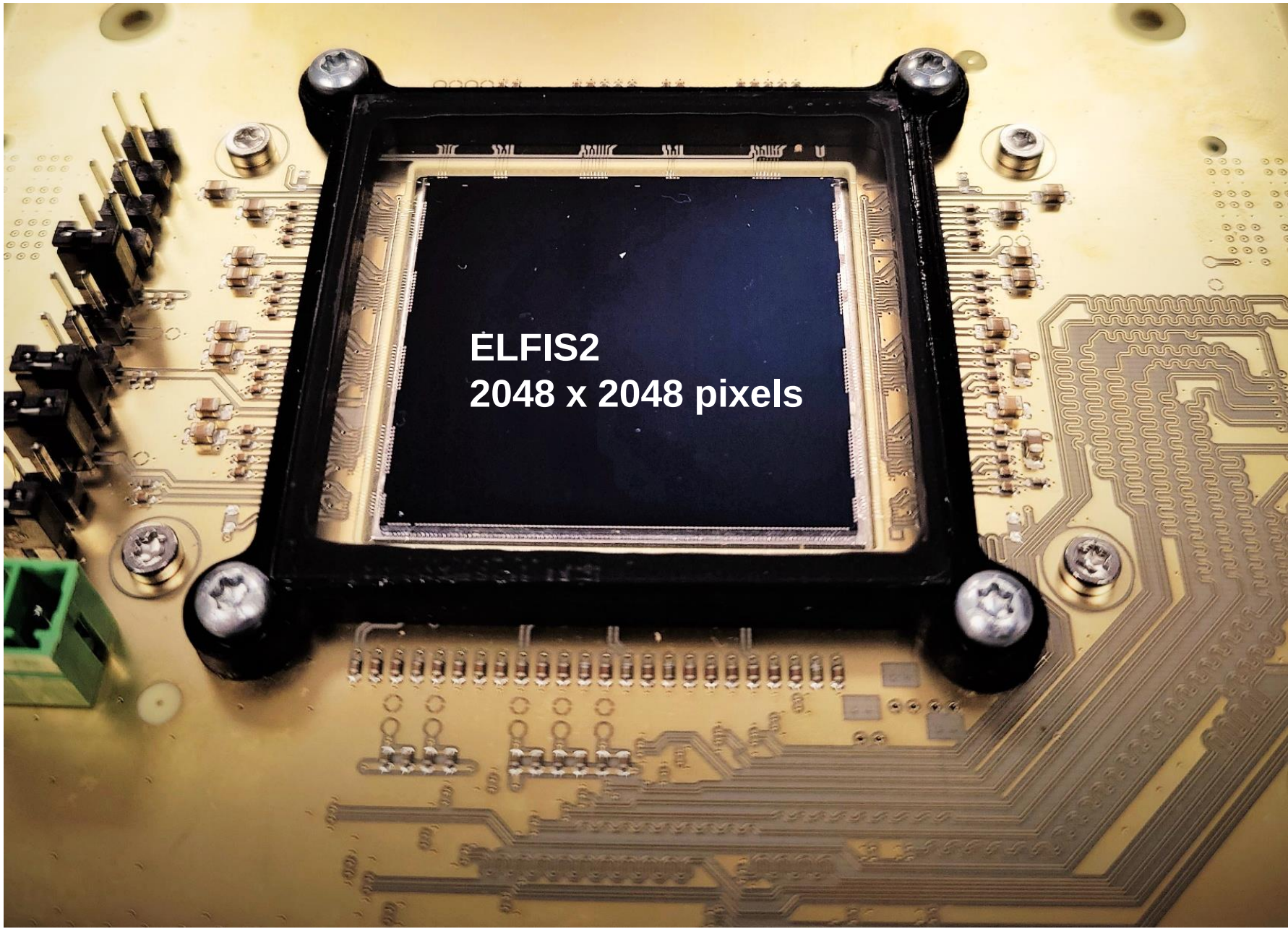
- Binning capabilities
  1. **Charge domain**
  2. Voltage domain

ELFIS2 is the successor of ELFIS
Dierickx & al,"A rad-hard, global shutter, true HDR, backside illuminated image sensor", Space & Scientific CMOS Image Sensors Workshop, Toulouse, 26-27 Nov 2019

Outline

1. Purpose
2. Key specifications
3. Charge domain global shutter and HDR
   - Concept
   - Measurement results
4. Charge domain binning
   - Concept
   - Measurement results
5. QE
6. Conclusions

ELFIS2 assembled chip on board [CoB]



Key specifications, measured

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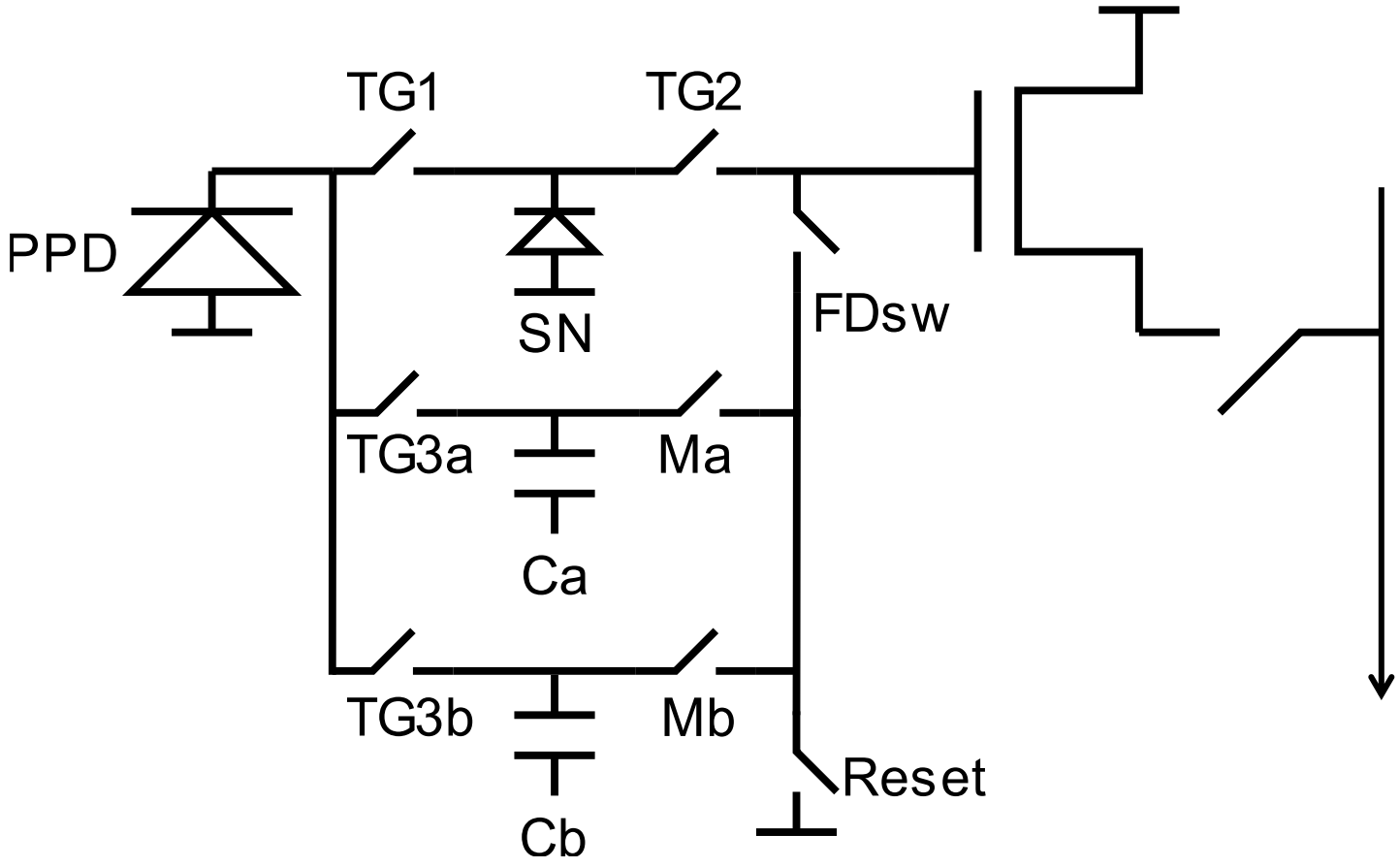
Stitching	✓
Stitch block size	1024 x 512
Possible resolutions	1024 x 512 **2048 x 2048** 9k x 9k
High gain Full well	13 ke^-
Low gain Full well (IWR)	180 ke^-
Low gain Full well (ITR)	360 ke^-
ROI in Y	✓
Read noise at nominal speed, GS	3.5 e_{rms}
FPN reduction	✓
Voltage domain binning	✓
Charge domain binning	✓
Low noise mode	✓

Back side illumination	✓
Backbias capability	✓
EPI thickness	6.5 µm, **12 µm, 22 µm** HIRES
QE for 22µm epi	~80% @ 400 nm ~85% @ 540-700 nm ~30% @ 1000nm
MTF	0.52 [12µm epi]
PLS	1/4000 at 630 nm 1/600 at 830 nm
Image lag	<0.5%
PPD dark current	< 500 e^-/s @ 33°C
Output channels for 2k*2k	16
Analog outputs	✓
Nominal channel rate	40 MHz
Frame rate for 2k*2k	150 fps

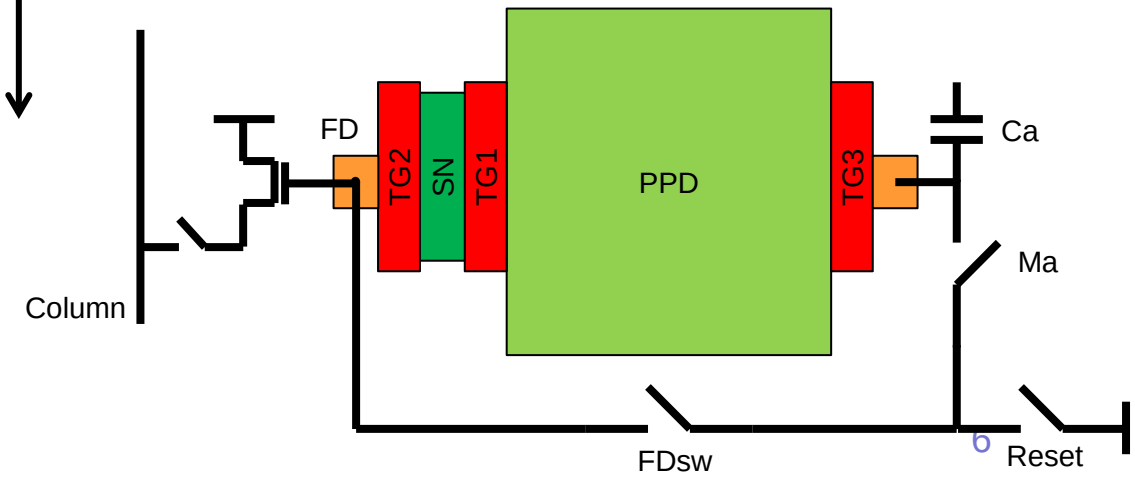
3.

Charge domain Global shutter and HDR

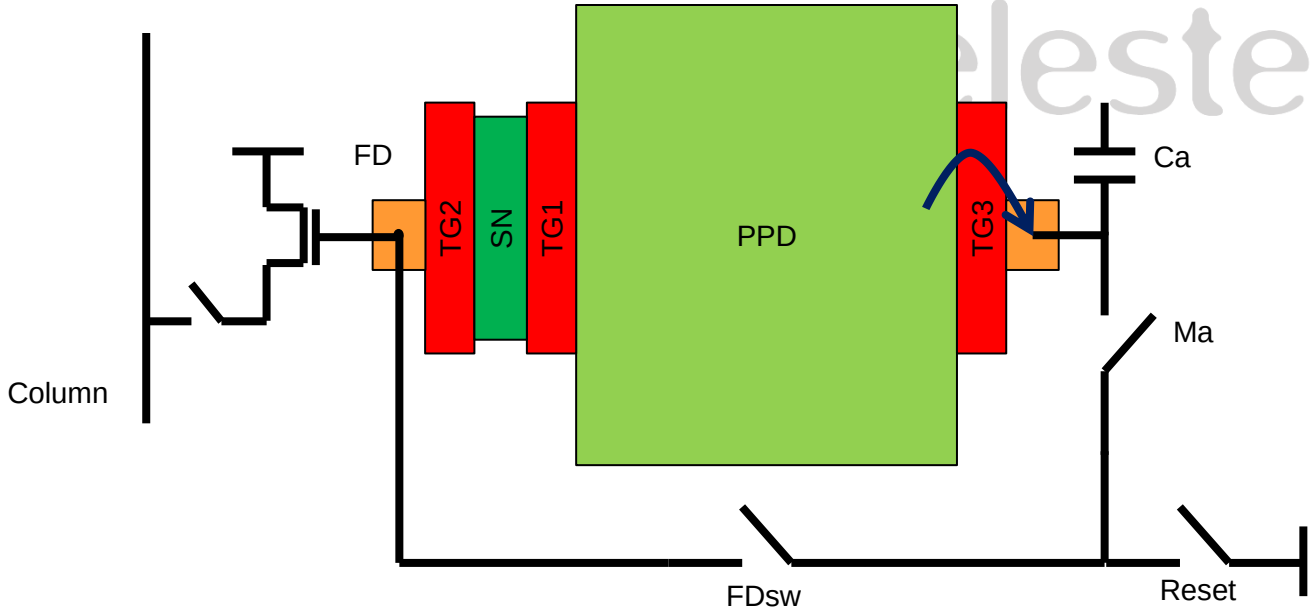
Charge domain Global shutter and HDR

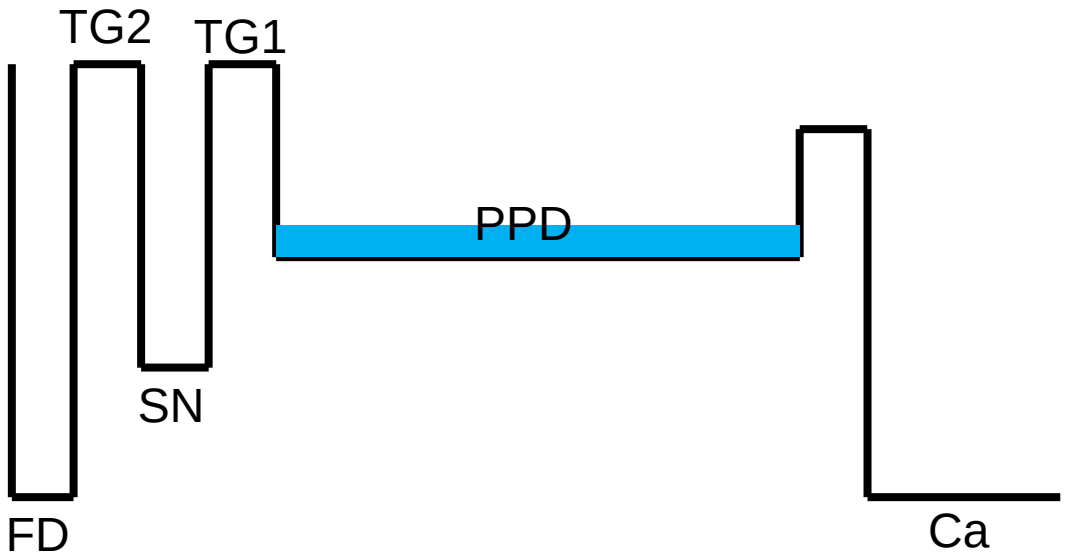


- During integration
  - charges overflow from PPD to Ca (or Cb) through TG3a (or TG3b)
- Global operations
  - PPD to SN through TG1
  - PPD to Ca through TG3a to transfer remaining charges
- Readout
  - High gain: SN to FD through TG2
  - Low gain: Averaging of FD and Ca

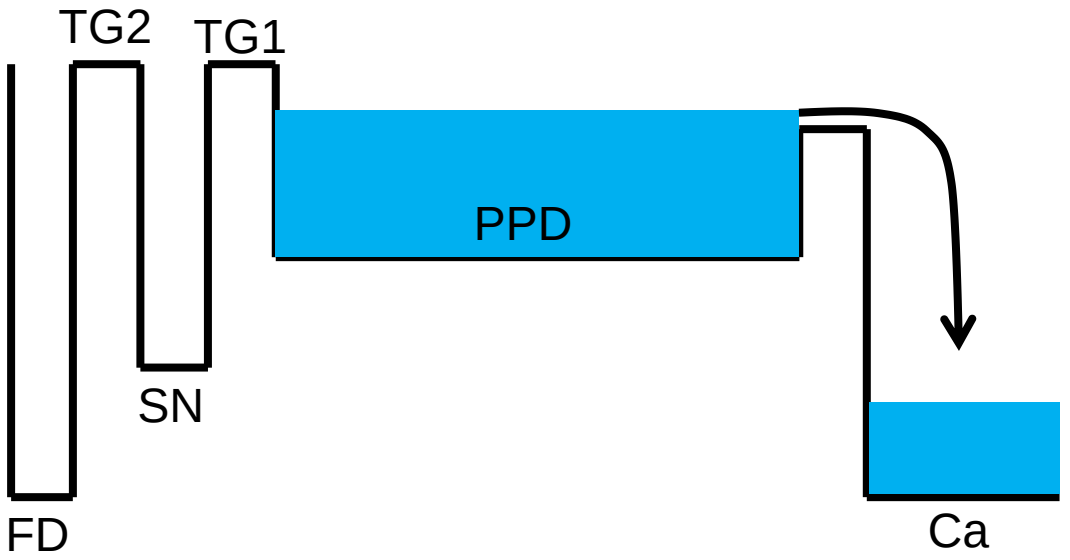


During Integration



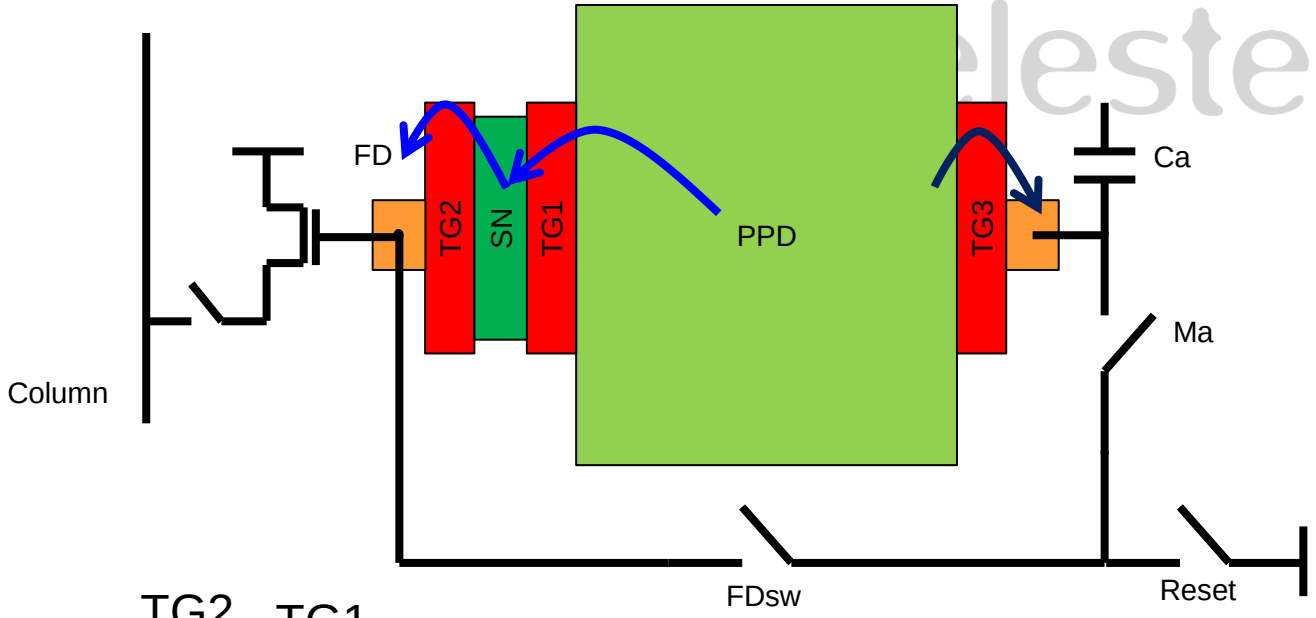


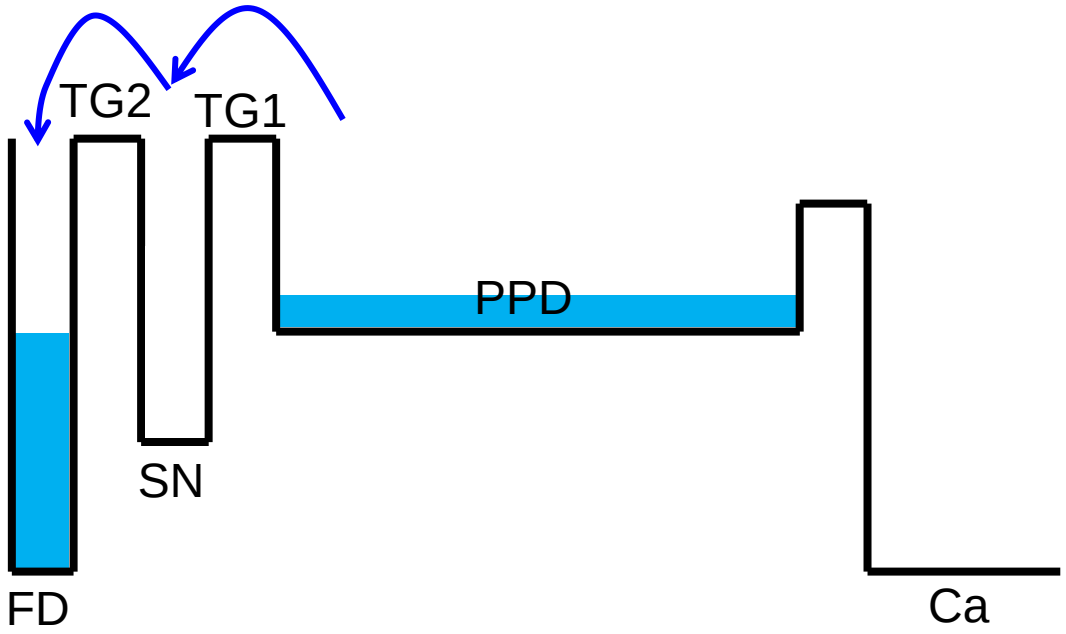
Low illumination:
Charges are contained in PPD

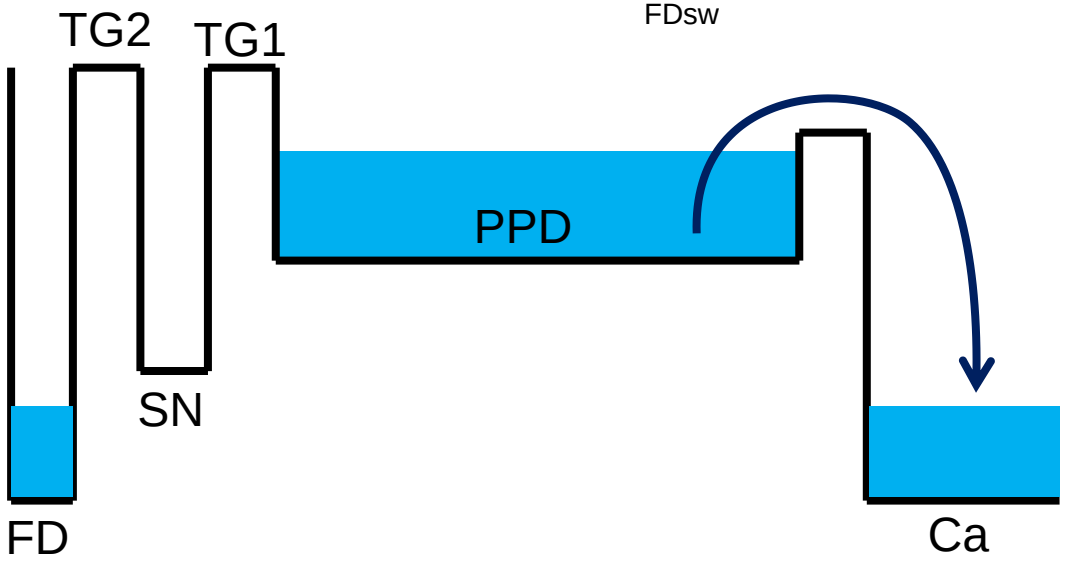


High illumination
Charges overflow to extra capacitor Ca or Cb

During Readout







Low illumination:

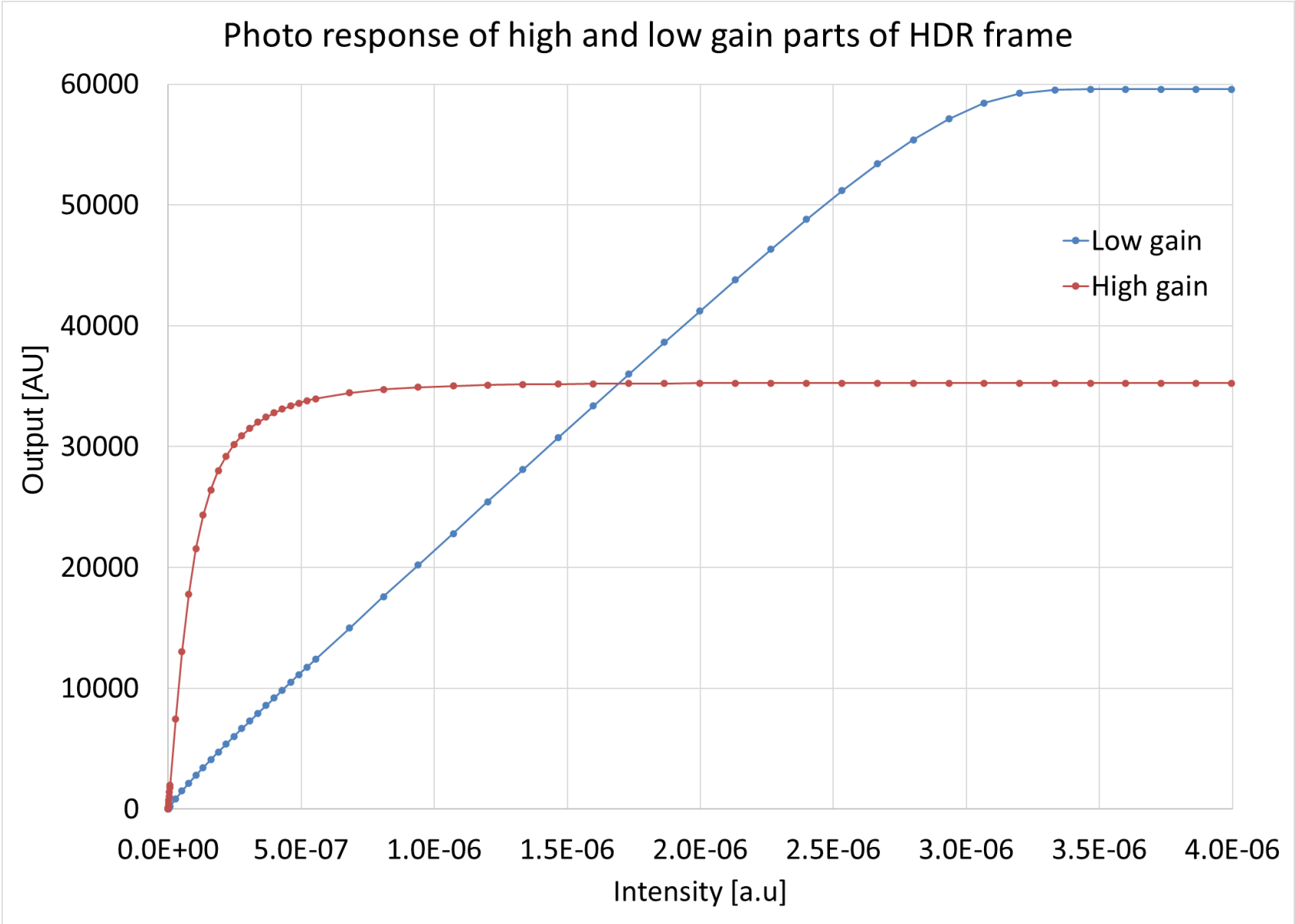
- High gain value after CDS is contains all information
- Ca is empty, low gain value is void.

High illumination:

- High gain value saturates
- Low gain value is the sum of Ca and FD

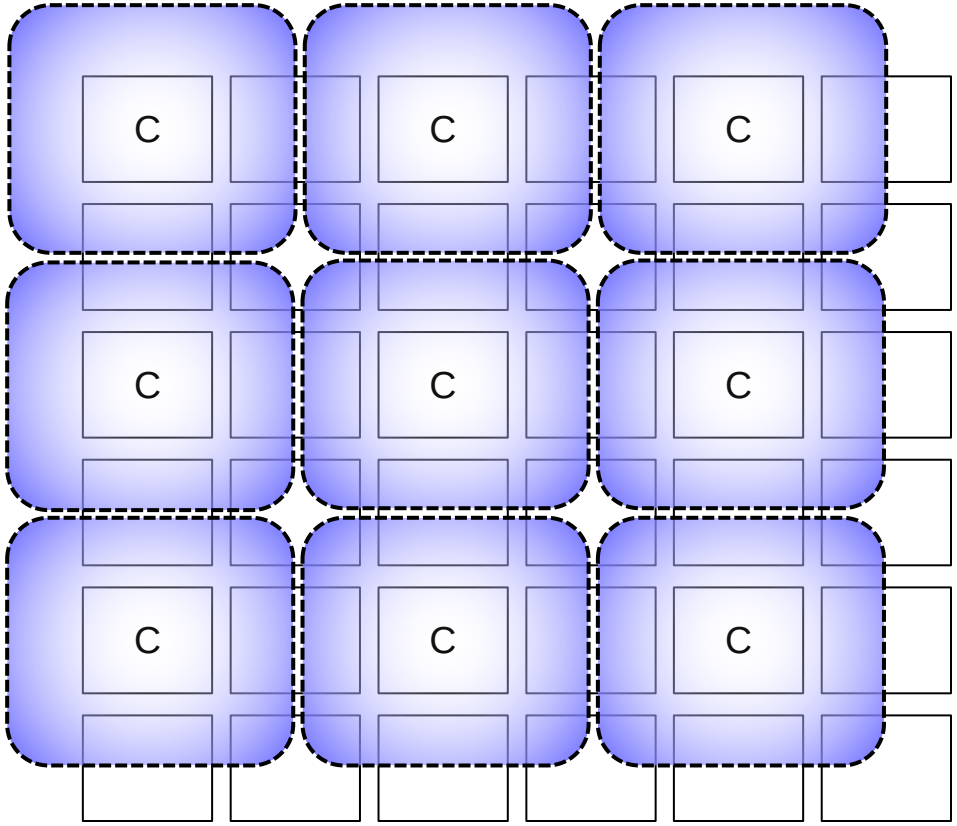
Measured Performance

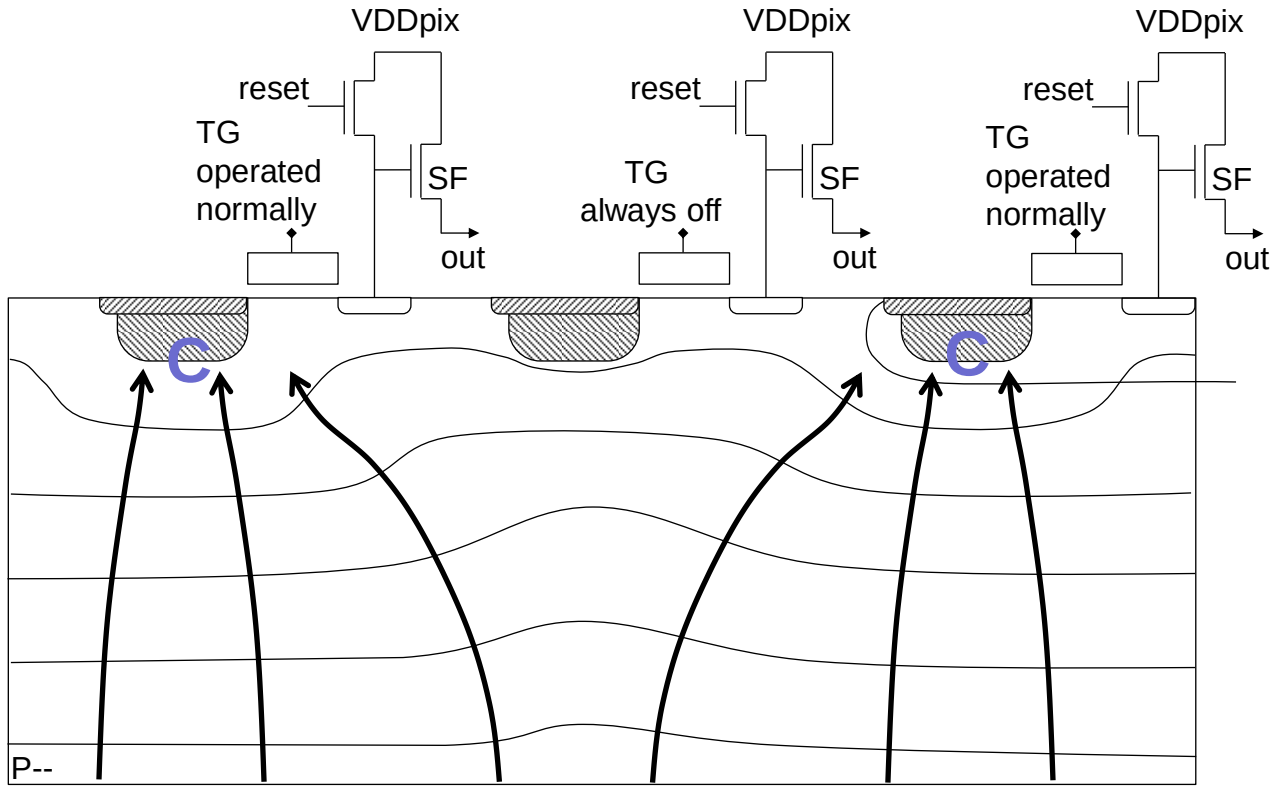
- High gain swing is limited by storage node capacity
- The overflow mechanism ensures high full well even with a PPD with low depletion voltage
- Obtaining HDR information
  - At low illumination levels, only high gain value is used
  - At high illumination only low gain information is used
  - The transition a weighted average of high gain and low gain values is used



4.
Charge domain binning

Concept of Charge domain binning





- In 2x2 configuration Pixel ‘C’ is intended to collect charges
- Others are in non-integrating state

Example implementation

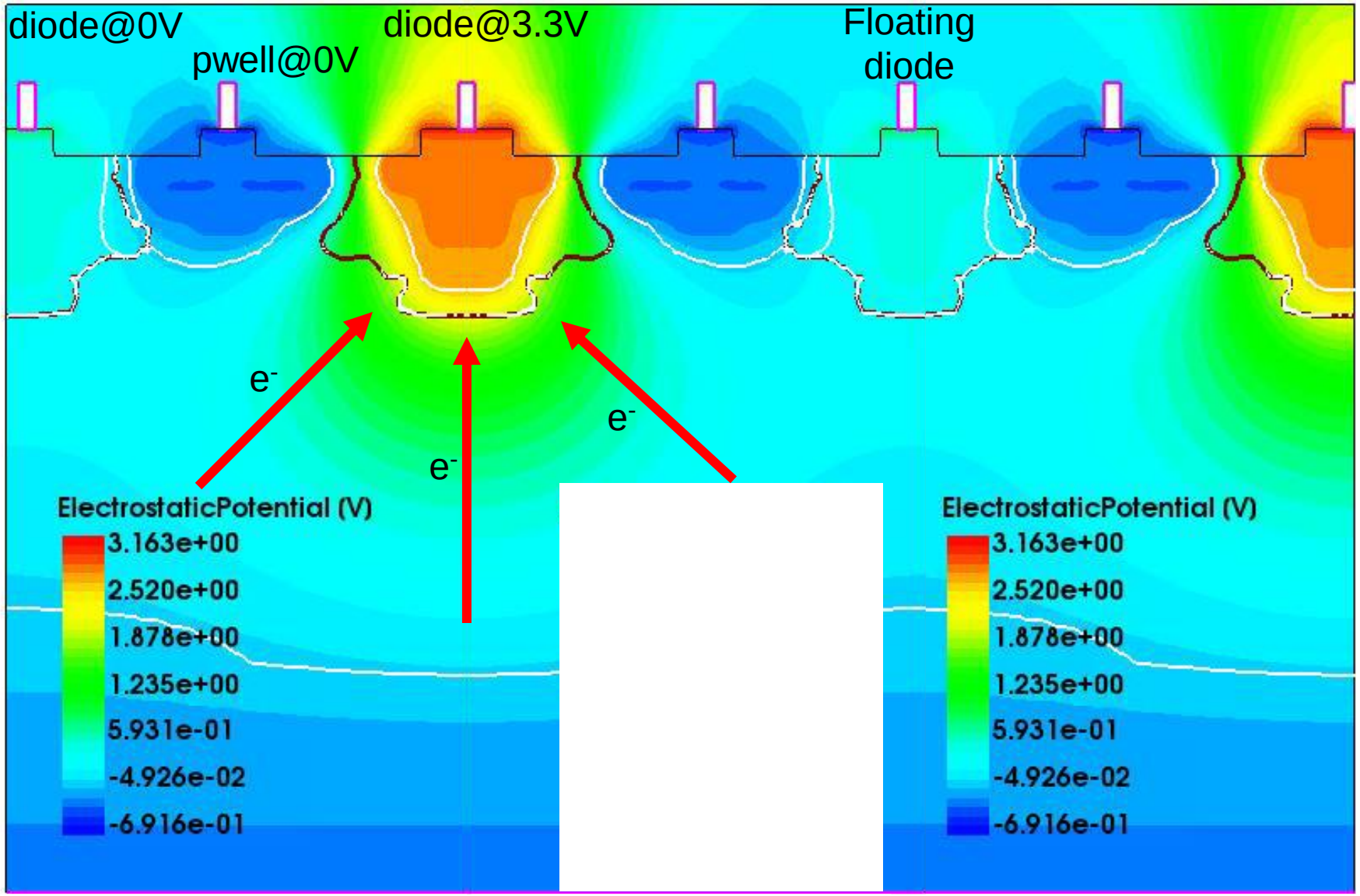
- The center PPD is never reset and thus floating
- PPD evolves to a non-integrating state.

TCAD Potential Profile, ideal case

- 12µm pitch
- 10µm thick HIRES epi (BSI)
- No backbias
- Illumination from backside
- Small diode (non PPD) @3.3V

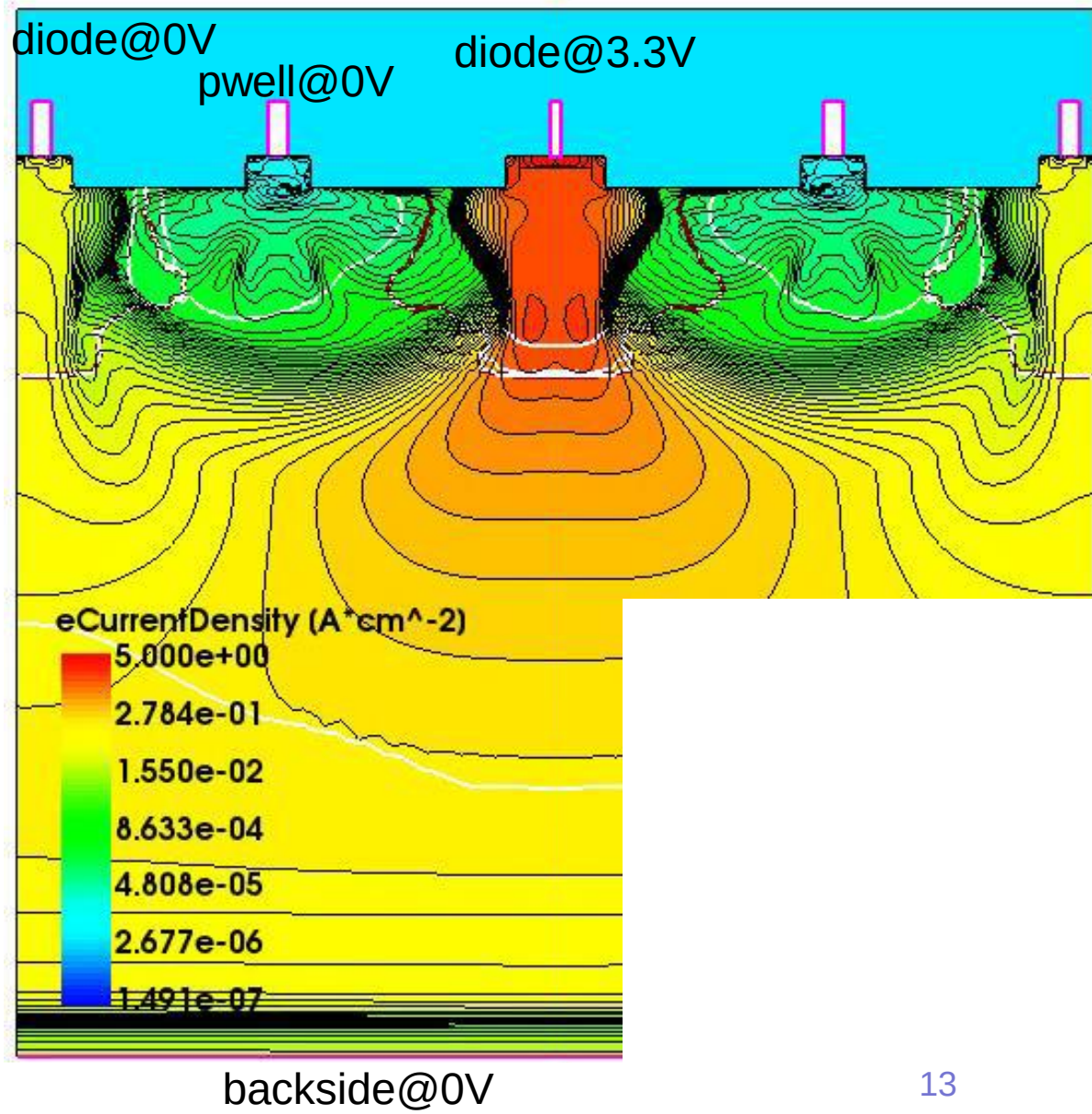
Observe significant tilt of equipotential lines.
Almost complete collection of backside charges in central diode for this simulation case.

Actual situation differs
- Real PPD
- Biased PPD $V_{depletion}$ is at +0.1V
- Floating diode is at -0.4V



TCAD Current density, ideal case

- Current density is highest towards the diodes biased at 3.3V while the diodes at 0V have almost no current flowing into them.

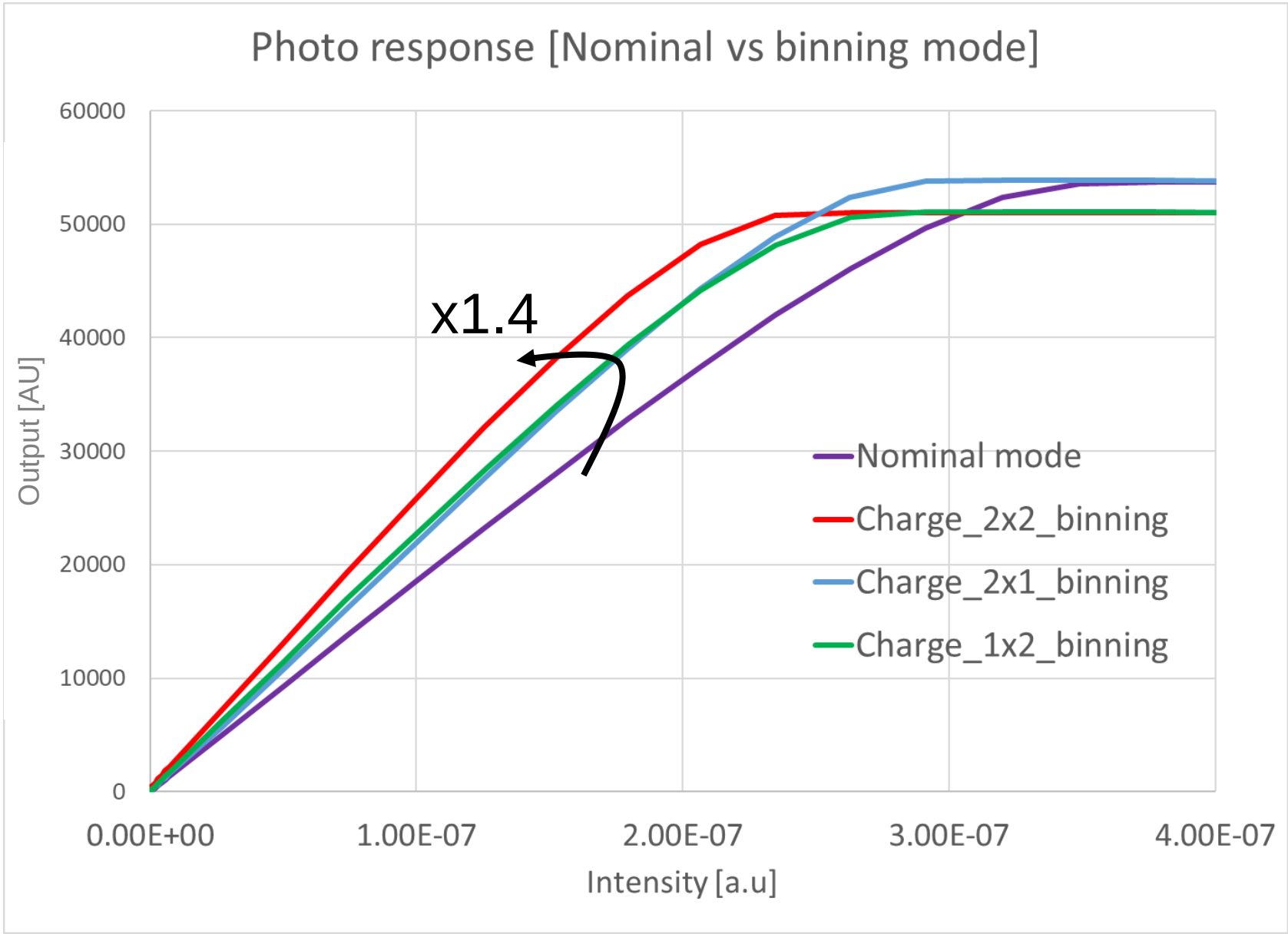


Measured Performance

- Binning concept works
- Performance is much less pronounced that in ideal case
- Ideal: binning has 4x higher response than nominal (non binned)
- Actual: binning has 1.4 times higher response than nominal mode

Reasons for reduced performance?

- ✓ Too small difference in potential between collecting and non-collecting diodes due to low depletion voltage. -0.4 V vs +0.1V.
- Recombination?
- Backside electric field distribution?

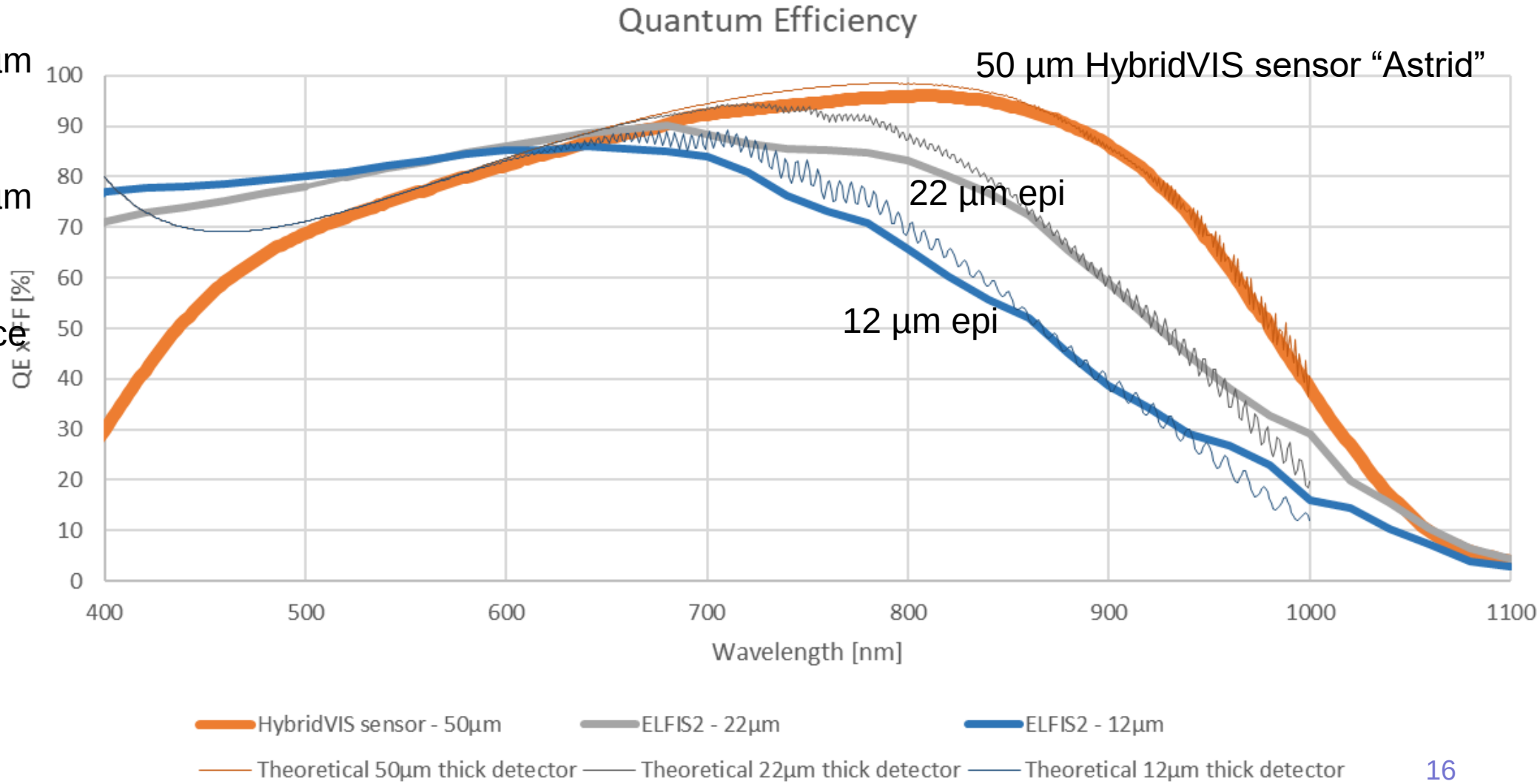


5.

Quantum Efficiency

Quantum Efficiency

- 58% QE at 900nm for 22µm epi
- 38% QE at 900nm for 12µm epi
- Close correspondence to model



Compare to ASTRID (HybridVIS, this workshop)

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5.
Conclusions

Conclusions

- Functionality of the 2k x 2k ELFIS2 sensor demonstrated
  - True High dynamic range: 360000e Q_{FW} / 3.5e Q_{noise} > 100dB
  - Motion artifact free global shutter combined with HDR
- Concept of charge domain binning in CMOS first time demonstrated, yet with lower efficiency
  - Lower performance probably caused by a low voltage difference between collecting and floating PPDs
- Excellent QE with BSI on 22 µm thick HIRES EPI wafer

- Further work
  - Behavior at Low temperatures
  - TID/SE radiation tests
  - Qualify low noise modes
  - On-chip FPN cancellation
  - Understand and improve charge domain binning