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A visible light and NIR hybrid CMOS image sensor

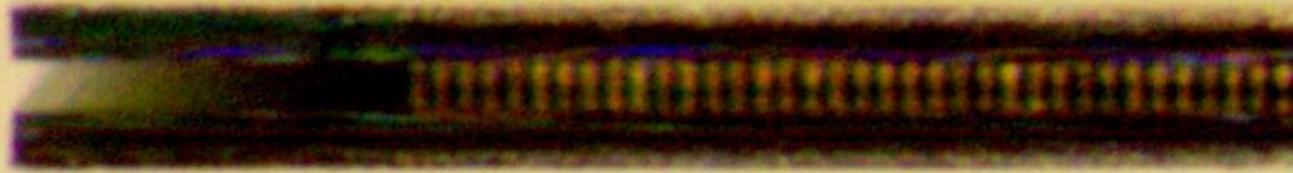
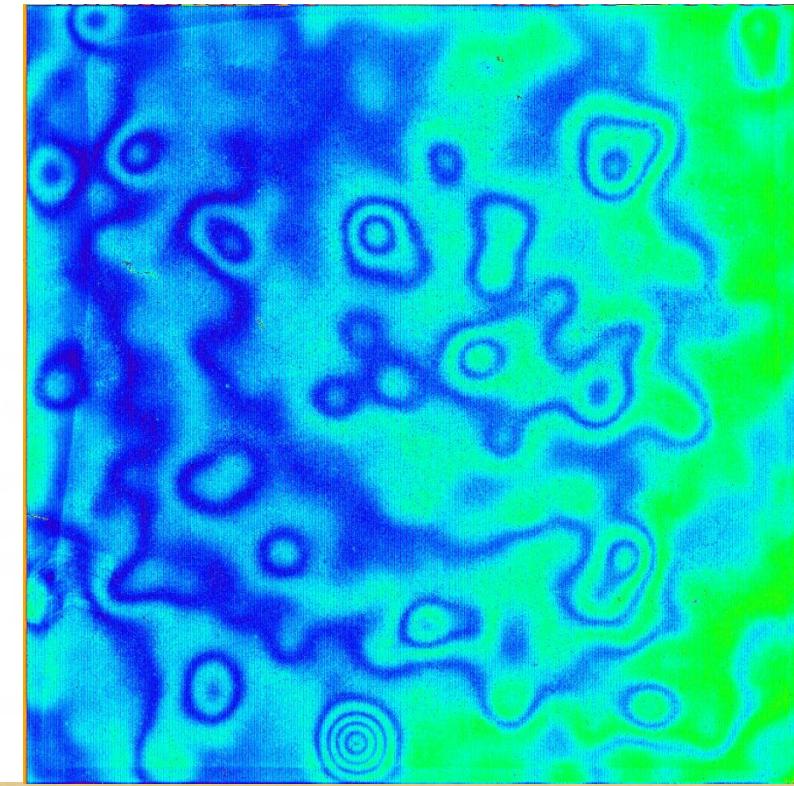
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workshop
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Outline

- Introduction
- Key specifications
- The pixel at ROIC-side
- The analog readout chain
- Detector layer
- Hybridization
- Electro-optical measurements
- Conclusions



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Introduction

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Hybrid image sensors are known from

- infrared imagers,
- X-ray detection,
- neural probes

Almost always this is the hybrid of a non-Silicon material to a Silicon ROIC.

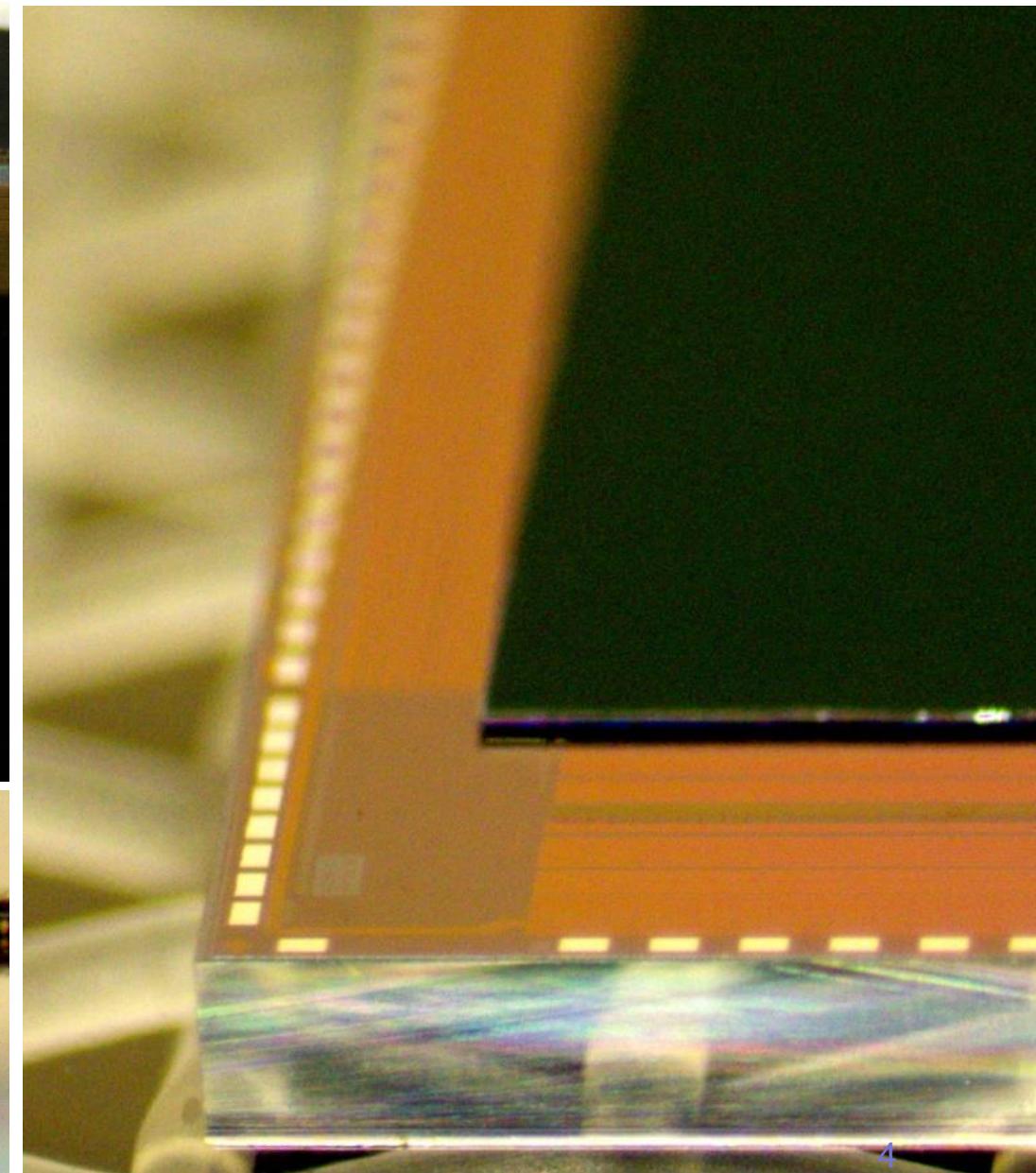
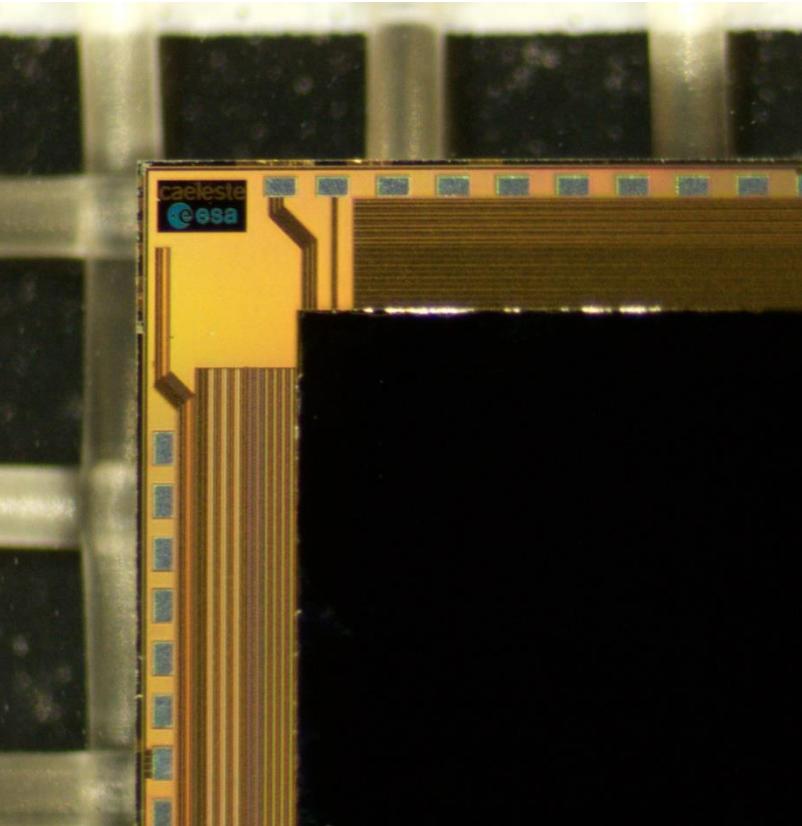
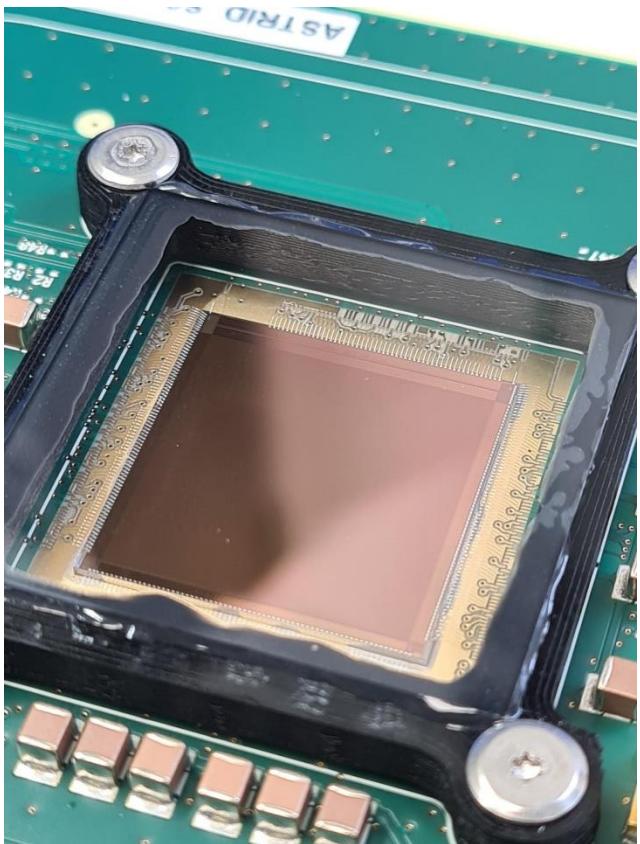
In this work we present a Si-Si hybrid: a Silicon detector layer on a Silicon ROIC.

Why?

- Best of both worlds, by independent optimization of
 - a plain CMOS ROIC
 - a very thick HIRES detector layer → strong electro-optical performance
 - Ultimate NIR response
 - Fill Factor of 100 %
 - Fully depleted pixels by independent substrate bias
- No thermal expansion mismatch problems, as with IR hybrids.

Introduction

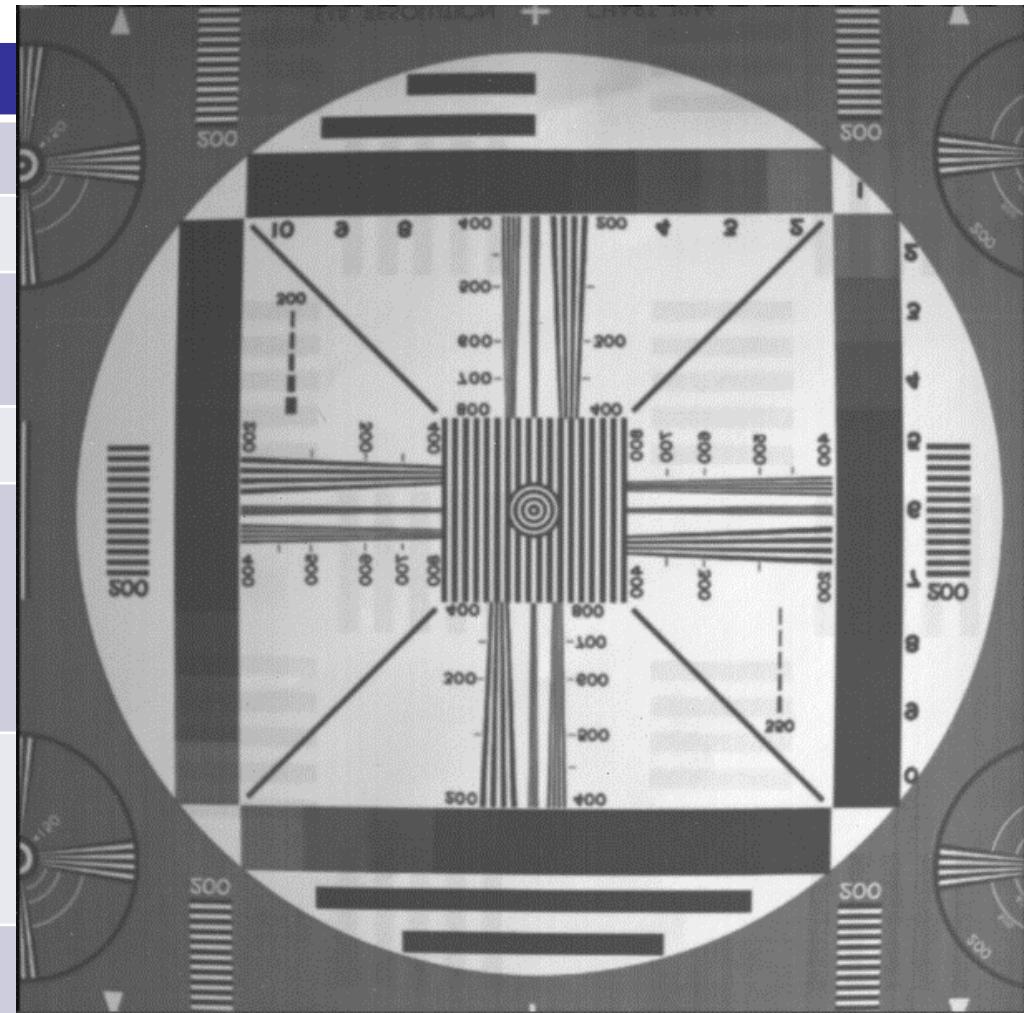
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Key specifications

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Parameter	Value
Number of pixels	1024 x 1024
Pixel size	20µm x 20µm
Readout modes	Global Shutter Rolling Shutter
Windowing	Y-direction
QE x FF 450nm - 950nm	> 50%
580nm – 920nm	> 80%
Peak @ 805nm	96%
Full well	[High Gain] 60ke ⁻ [Medium Gain] 300ke ⁻ [Low Gain] 1.2Me ⁻
Read noise [High Gain]	36 e ⁻ _{rms}
Low noise modes	Column gain, Non-Destructive Readout
Radiation hardness	TID 20krad Proton fluence 1×10^{11} protons/cm ²
Frame rate	40Hz (4 output channels @ 15MHz)



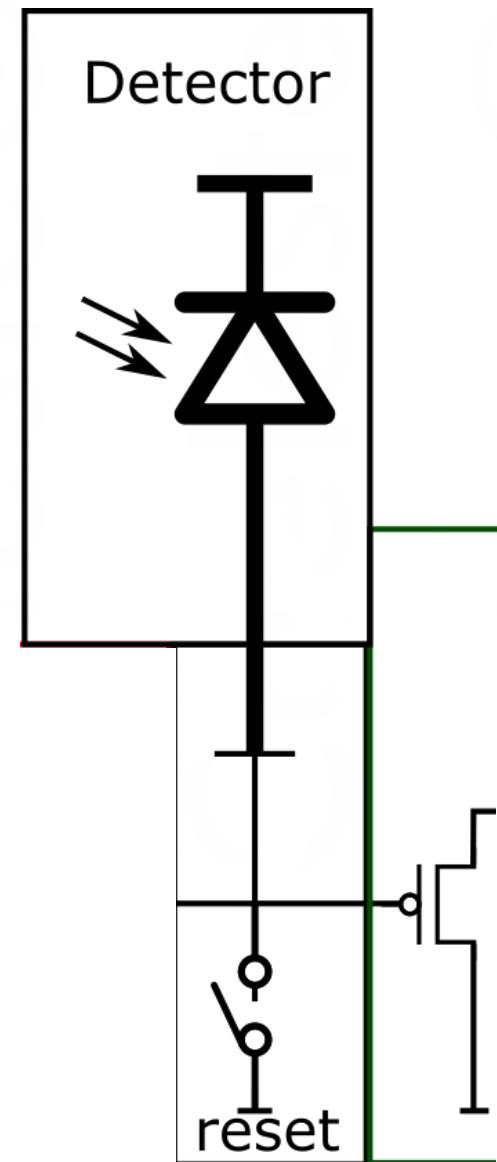
The pixel at the ROIC-side

Core: 3T pixel

3-level HDR

- High Gain: 60ke^-
- Medium Gain: 300ke^-
- Low Gain: 1.2Me^-

Global shutter by in-pixel memory



The pixel at the ROIC-side

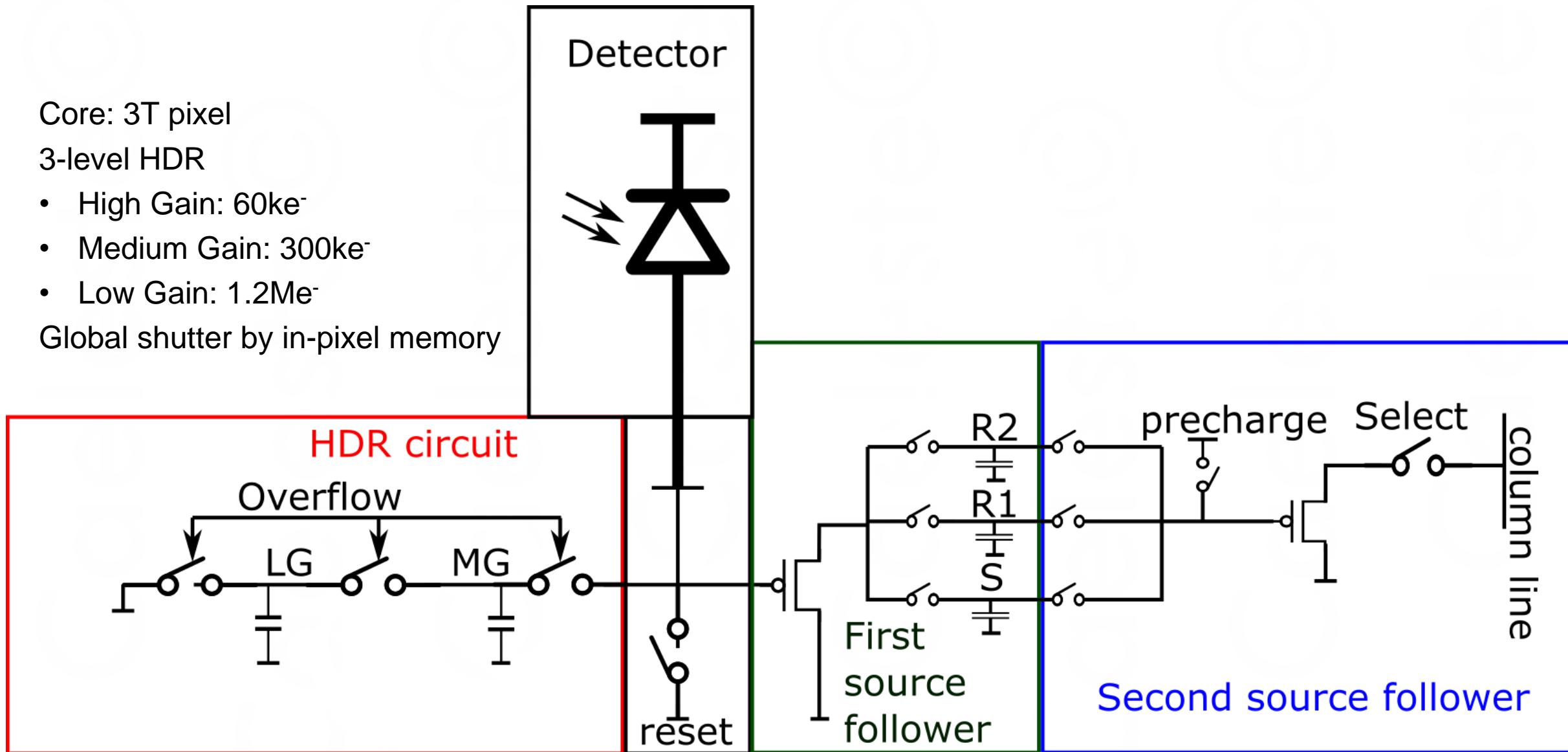
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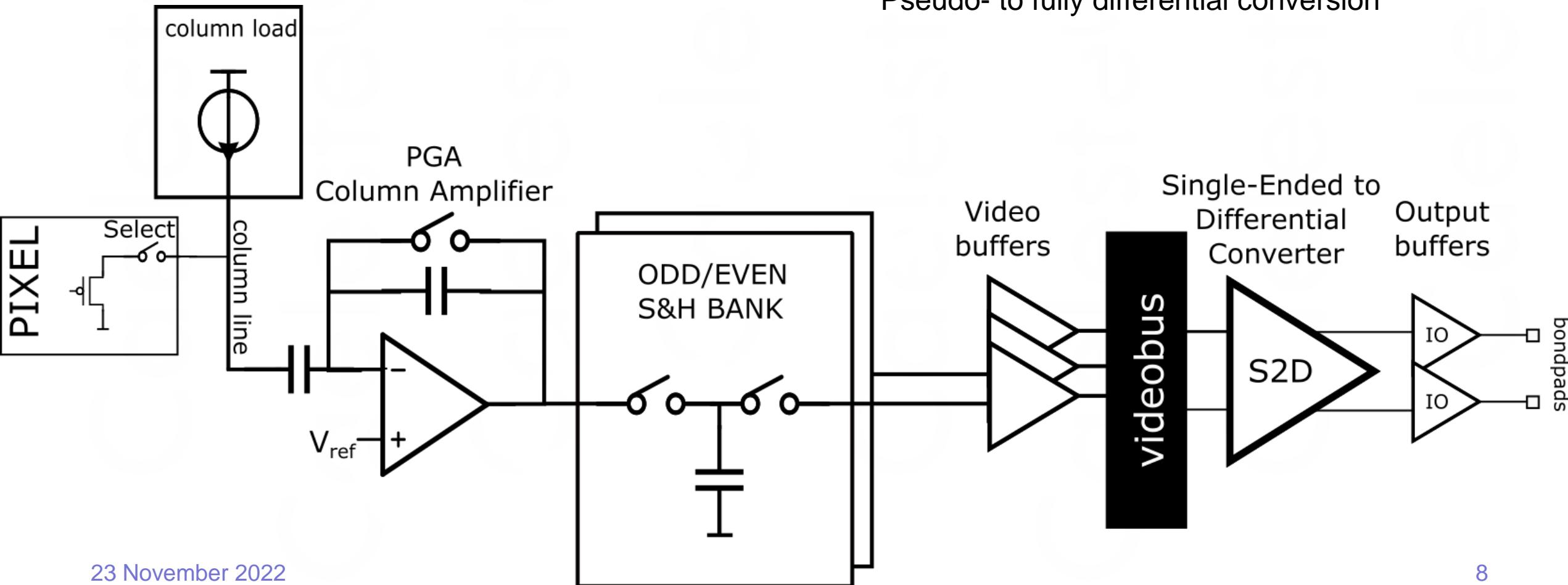
Global shutter by in-pixel memory



Analog readout chain

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Programmable column gain [x1, x2, x4]
Odd/Even row readout for parallelization
Video bus multiplexing
Pseudo- to fully differential conversion



The pixel at ROIC-side

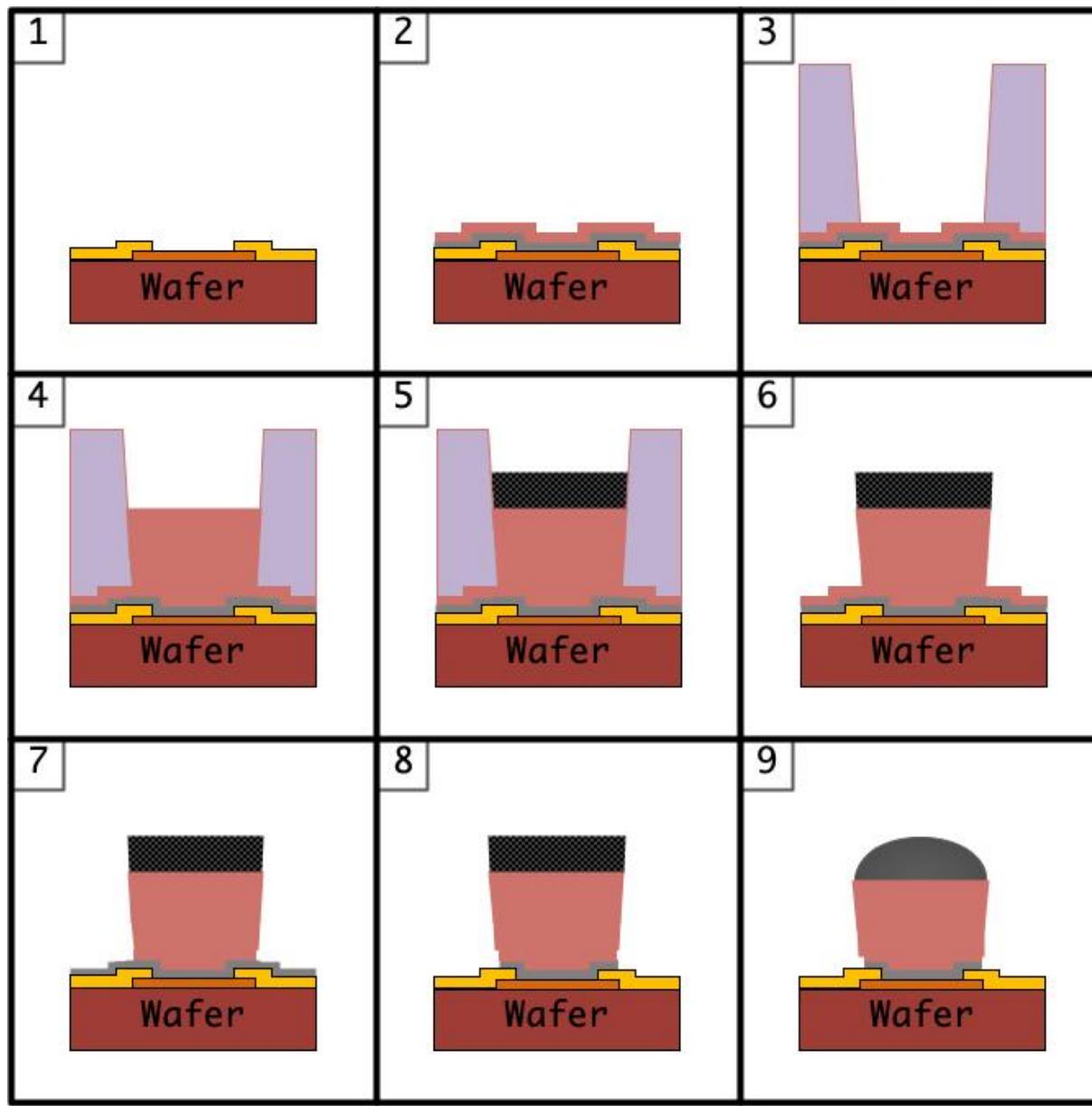
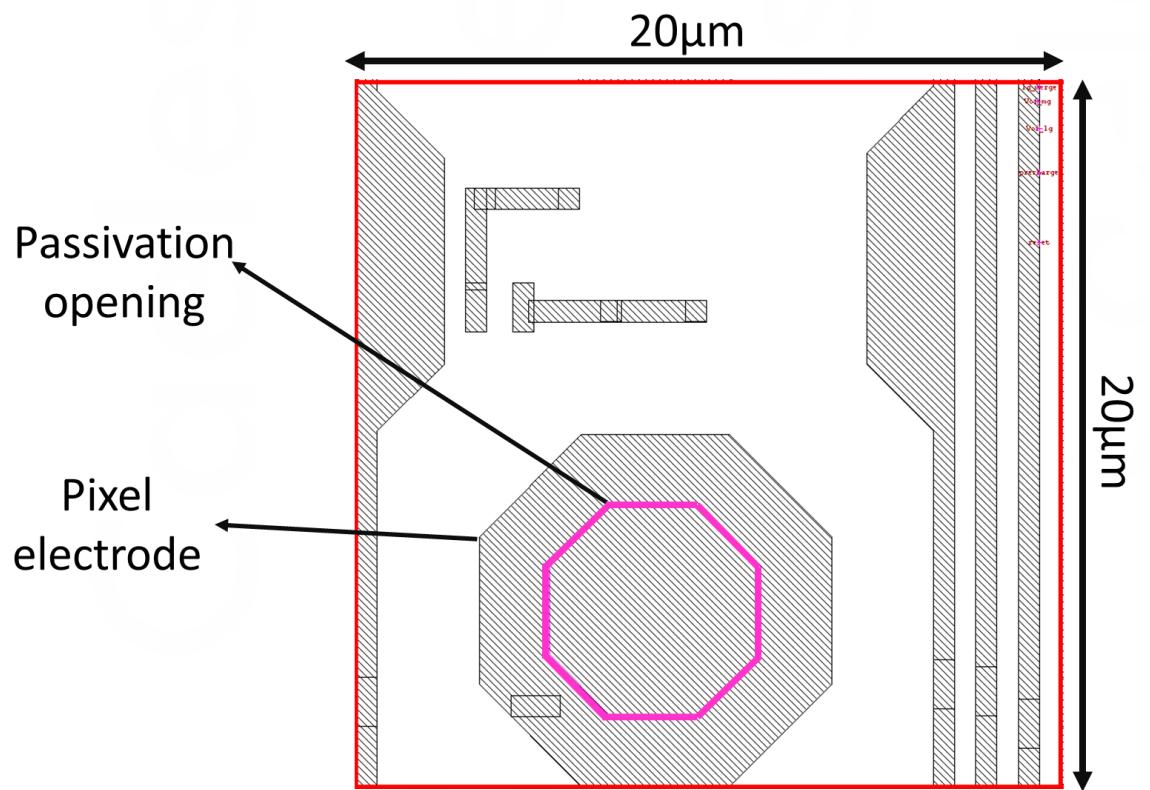
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ROIC-side contains a pixel electrode

Passivation is opened above this pixel electrode

Pillar is grown from this ROIC-side opening

Solder caps at top of pillar



Detector layer

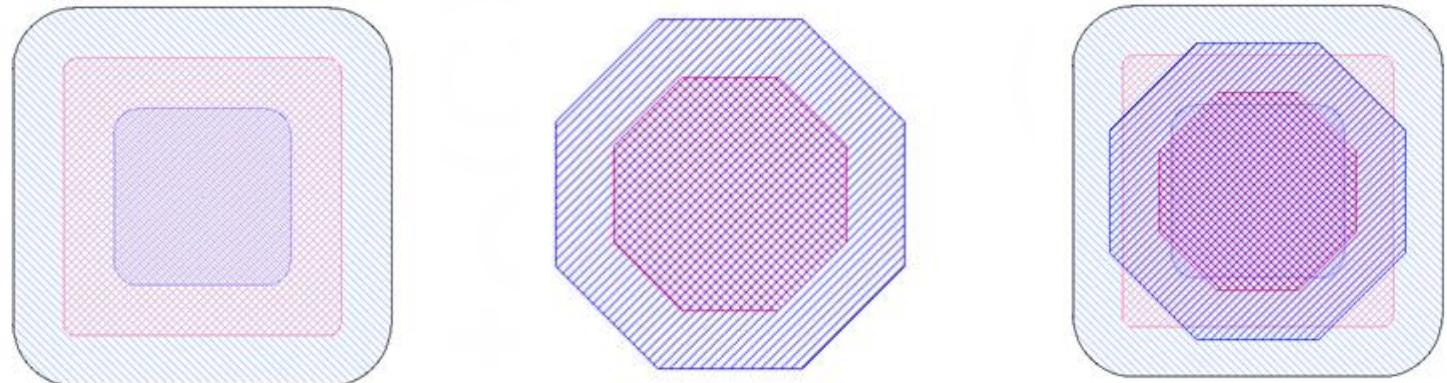
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high resistivity Si wafers

- ~15kOhm-cm
- 50 μ m thick

Solderable

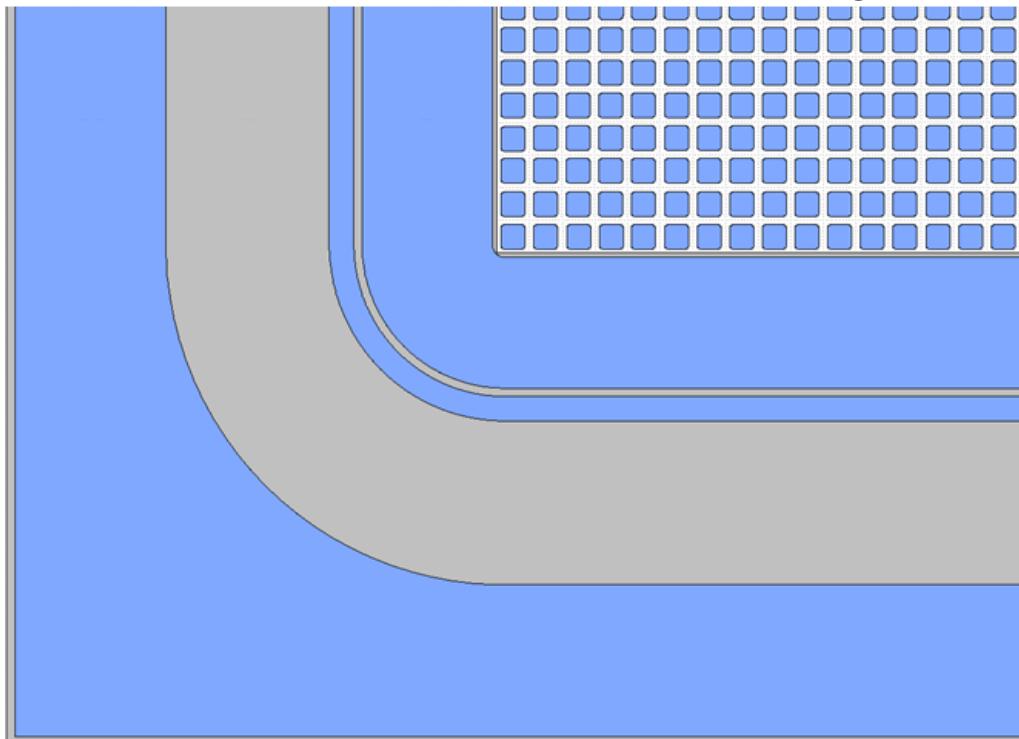
Under-Bump Metallization (UBM)
pads at each pixel pad.



Metal, implant & contact

UBM &
passivation opening

All layers

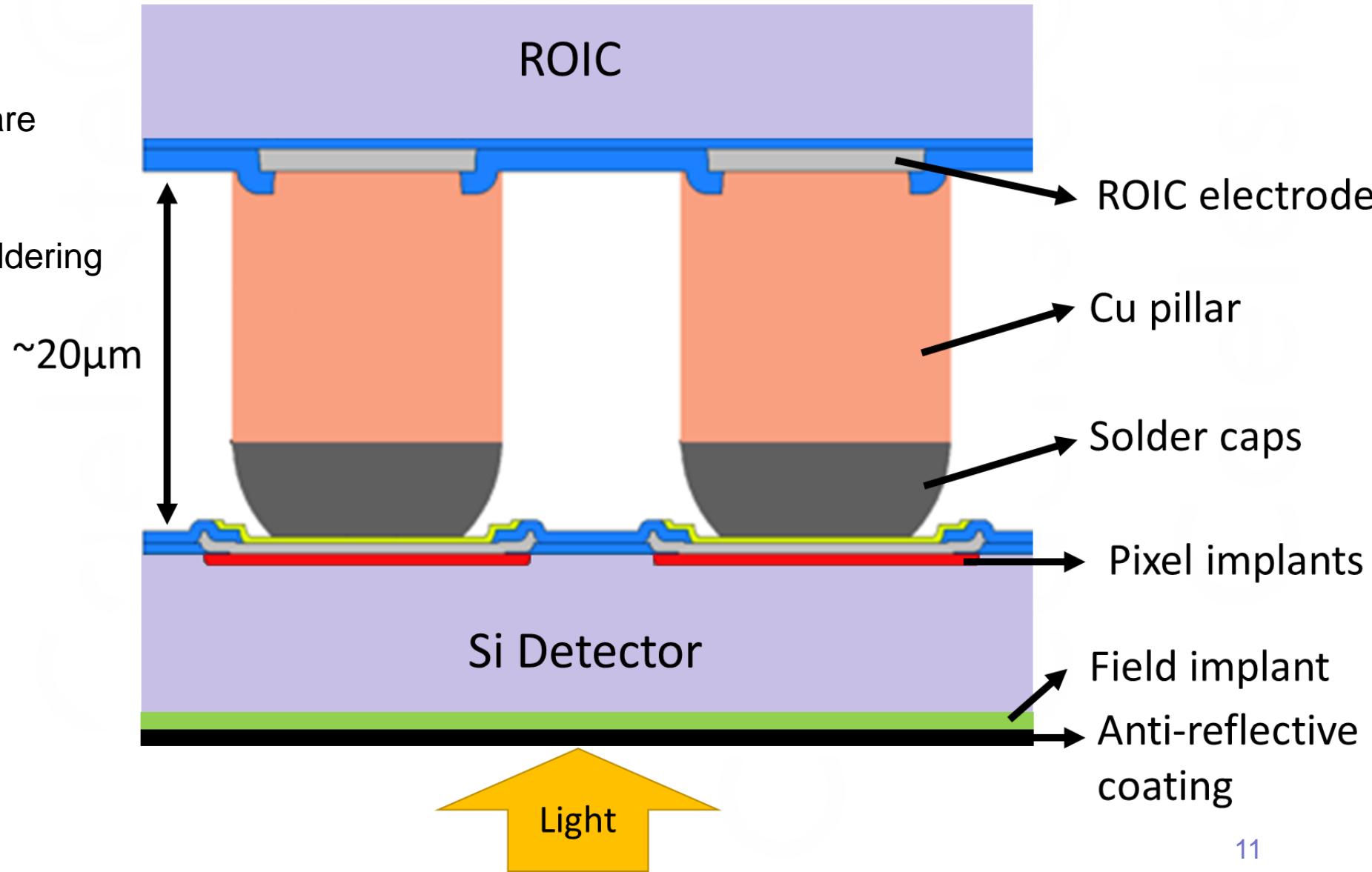


Hybridization

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Solder caps on ROIC pillars are the flip-chip interconnects

UBM at Si Detector allows soldering



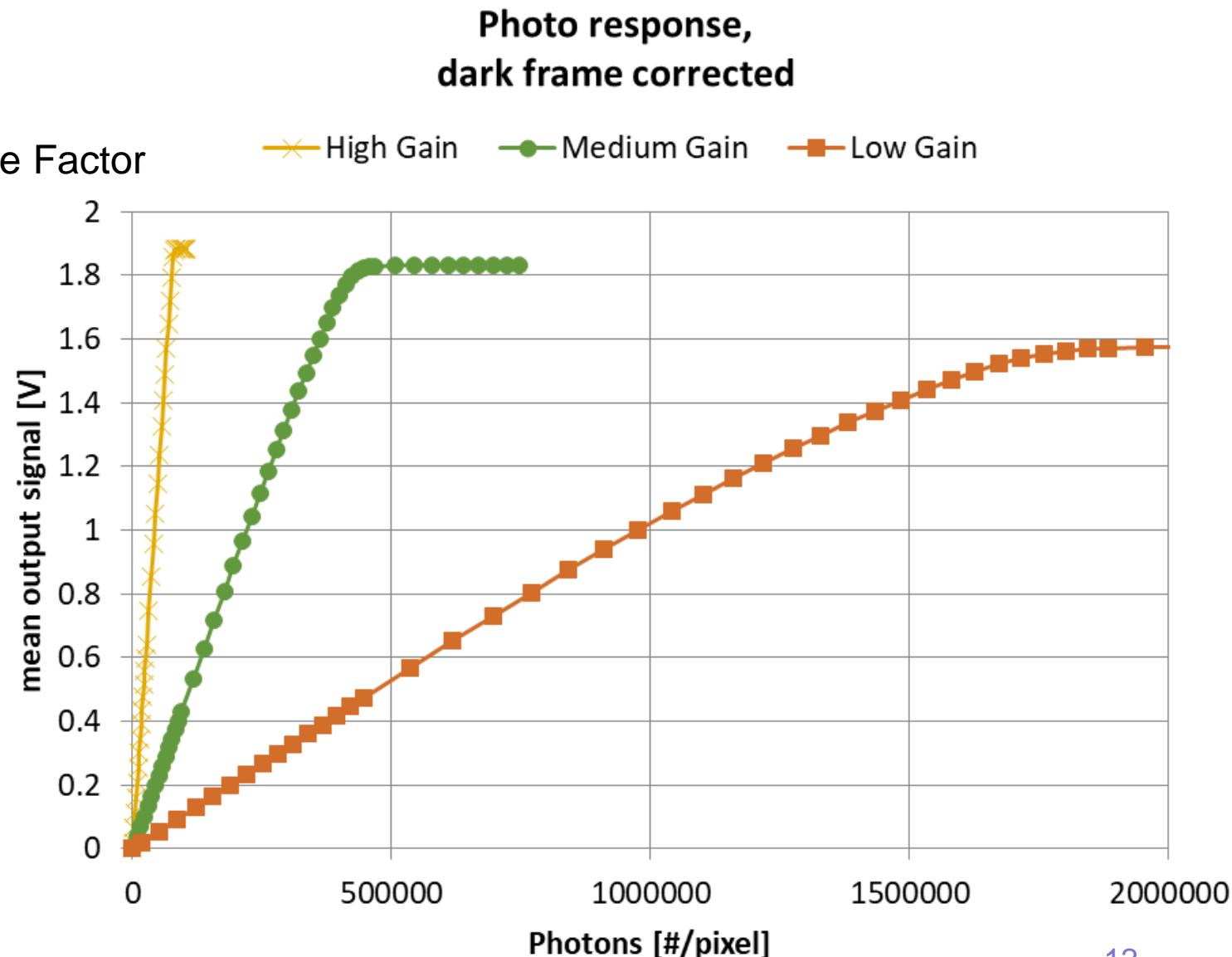
Electro-optical measurements

- photo response

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Photo response for 3 available pixel gains
Showing off full well and Charge-to-Voltage Factor

- High Gain
 - Full well: 58.4 ke^-
 - CVF: $32.2 \mu\text{V/e}^-$
- Medium Gain
 - Full well: 302 ke^-
 - CVF: $6.1 \mu\text{V/e}^-$
- Low Gain
 - Full well: 1.18 Me^-
 - CVF: $1.3 \mu\text{V/e}^-$

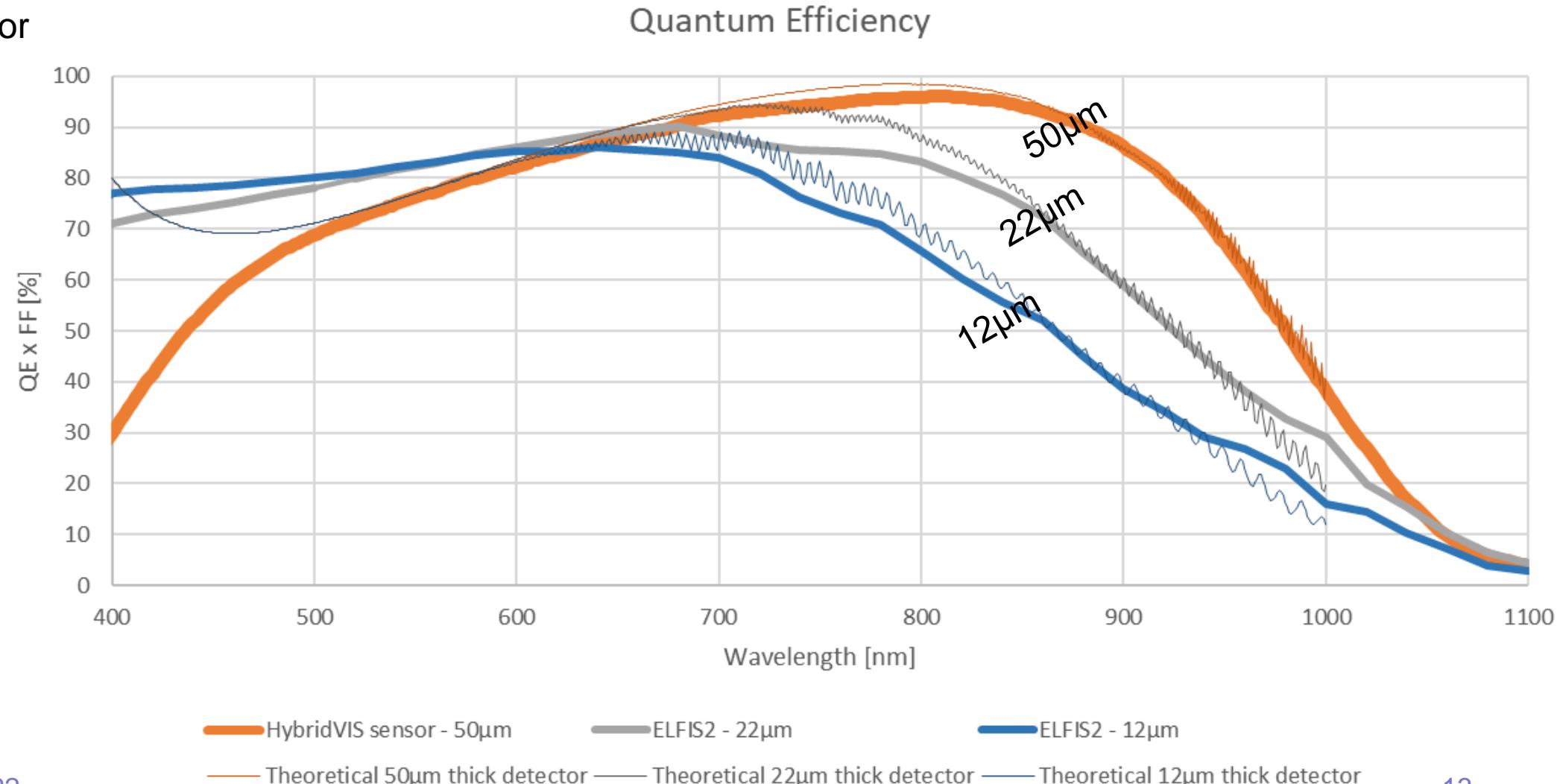


Electro-optical measurements - QE

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Comparison between theoretical & observed QE for

- Hybrid sensor (50 μm thick detector)
- ELFIS2 sensor
 - 22 μm
 - 12 μm



Electro-optical measurements

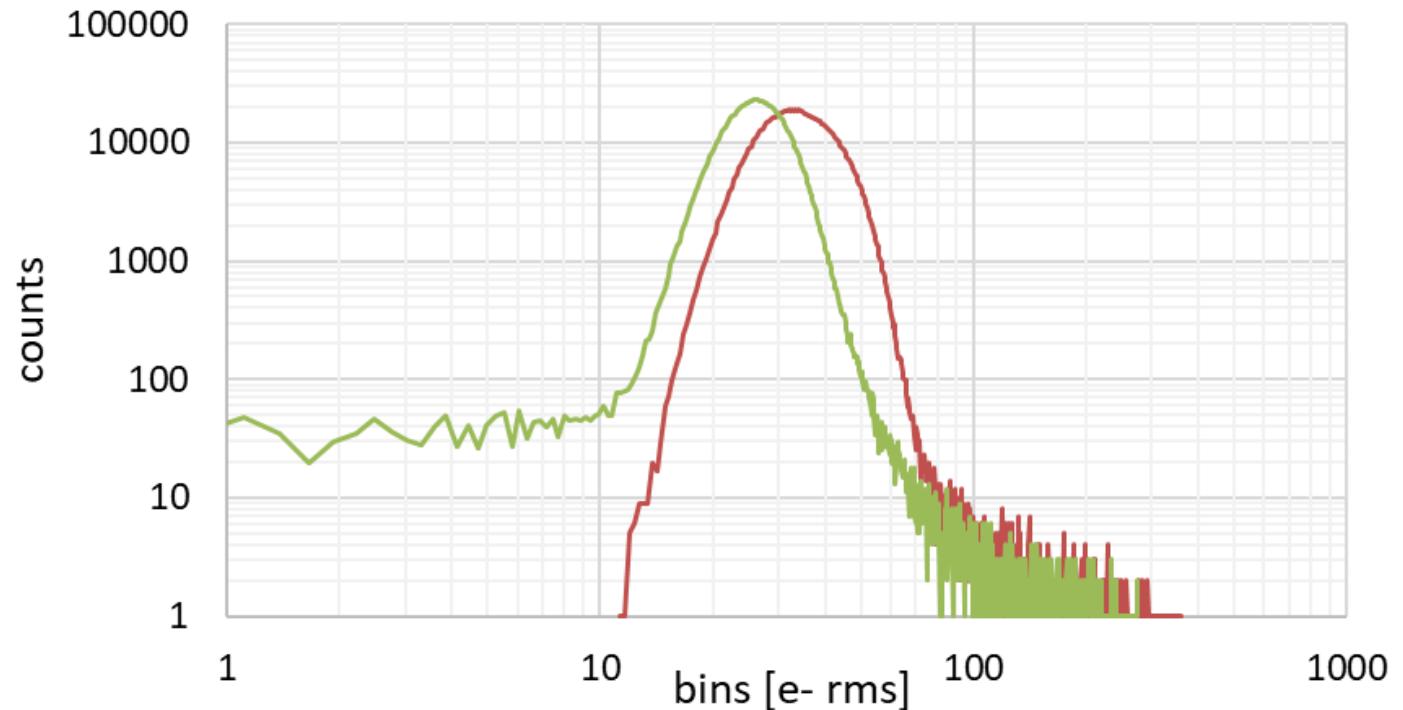
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- Noise

For a $C_{FD} = 9.9\text{fF}$

Noise histogram with different column gains
Correlated Double Sampling

- High pixel Gain - Column Amplifier Gain 1
- High pixel Gain - Column Amplifier Gain 4



Read out mode	Column gain	noise [e^-_{rms}]
Correlated Double Sampling	1	36
	4	28

Conclusion

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Demonstrated manufacturability of hybrid Si-Si sensor module for visible & NIR light

Advantages compared to monolithic sensor:

- Improved Near-InfraRed QE due to thick Si Detector wafer options
- Straightforward fully depletion by independent resistivity & biasing of the detector Si-wafer
- Essentially BSI Fill Factor quality

Disadvantages compared to monolithic sensor:

- Limited to 3T-pixel topology, no true CDS as in 4T-pixels
- Decreased sensitivity (CVF), inherent to hybrid architectures
- Keep eye on mechanical stability of the modules
- Multiple additional steps required in production

Future work

- Evaluating low noise modes (NDR, ...)
- MTF, Parasitic Light Sensitivity
- Qualification

Questions?

