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Astronomy Large Format Array Controller (aLFA-C): design and characterization of an advanced FPA controller

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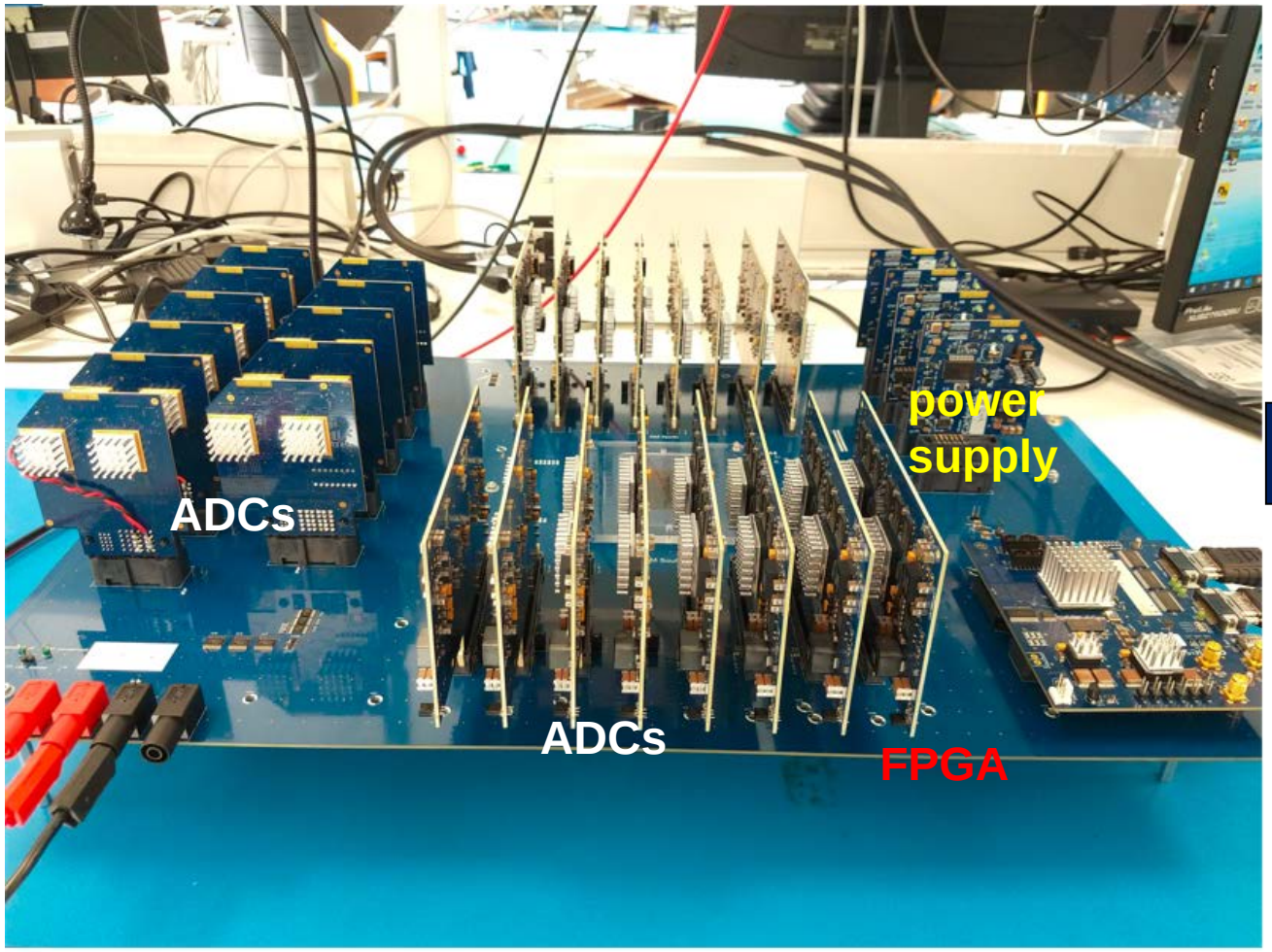
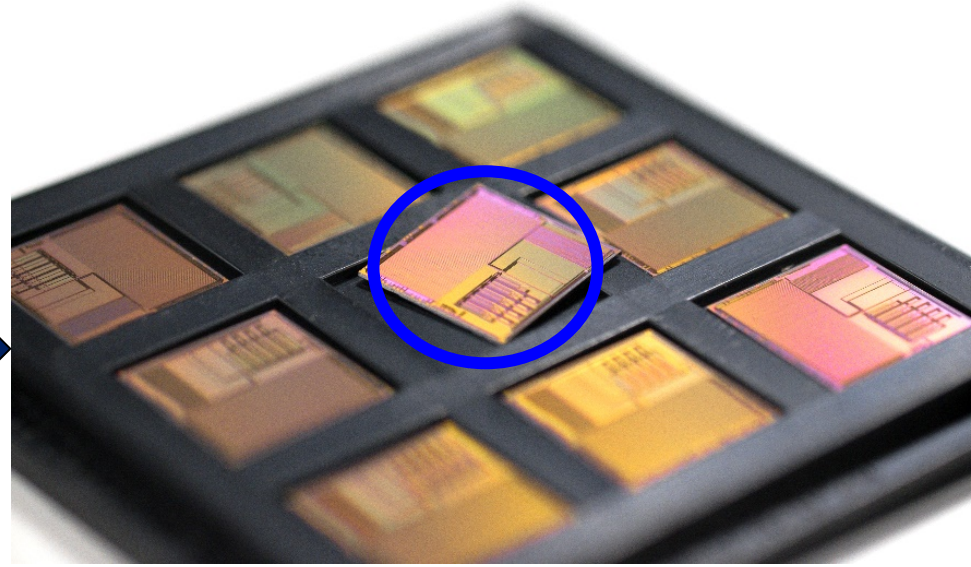
Outline

- Motivation
- Architecture
- Building blocks design
- Test results
- Conclusions

Motivation





Space application: compact, lower power

Functions and challenges

aLFA-C ASIC: For future space astronomical science missions

- **Analog domain**
  - Signal conditioning
  - A/D converter
  - Regulated power supply
  - Bias voltage/current references
  - House keeping
- **Digital domain**
  - Sequencer
  - Memory
  - SpaceWire

Environmental constraints:

SPACE

- Radiation
- High reliability

INFRARED

- Operating close to the focal plane temperature e.g. << 77K

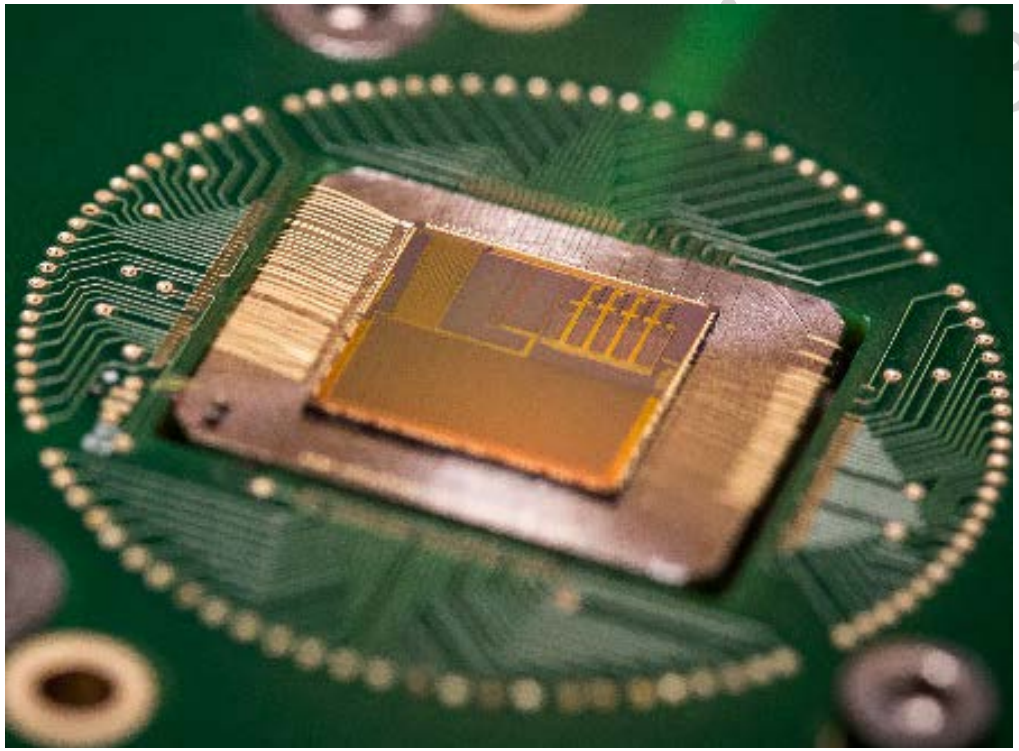
Development status

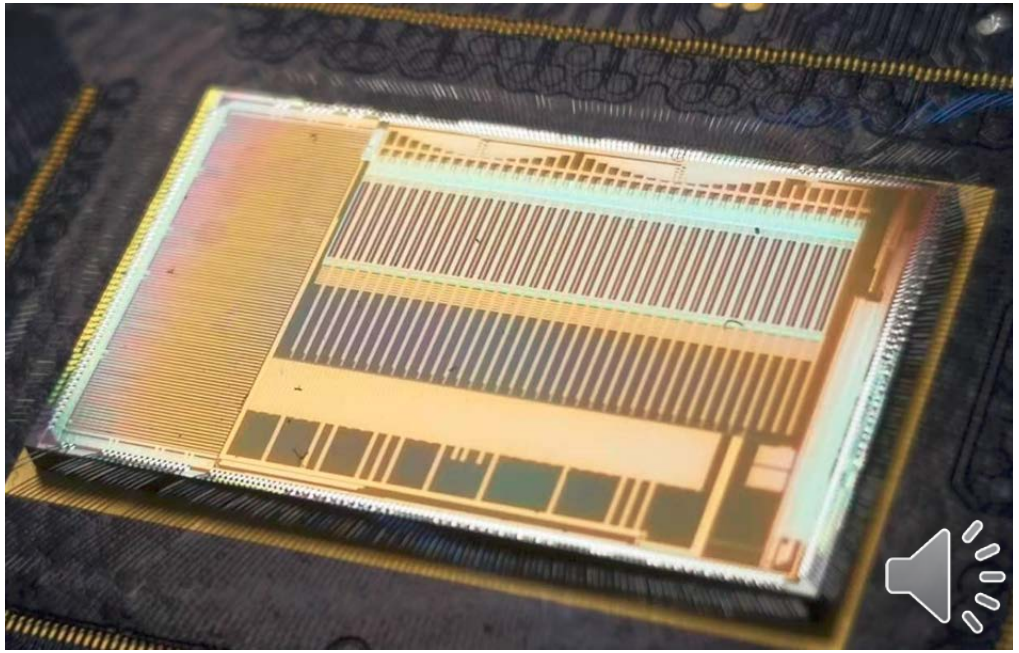
aLFA-C: prototype (2014)

- 16-bit SAR ADCs
- Programmable sequencer
- Memory cells
- All key building blocks perform well at RT and 77K

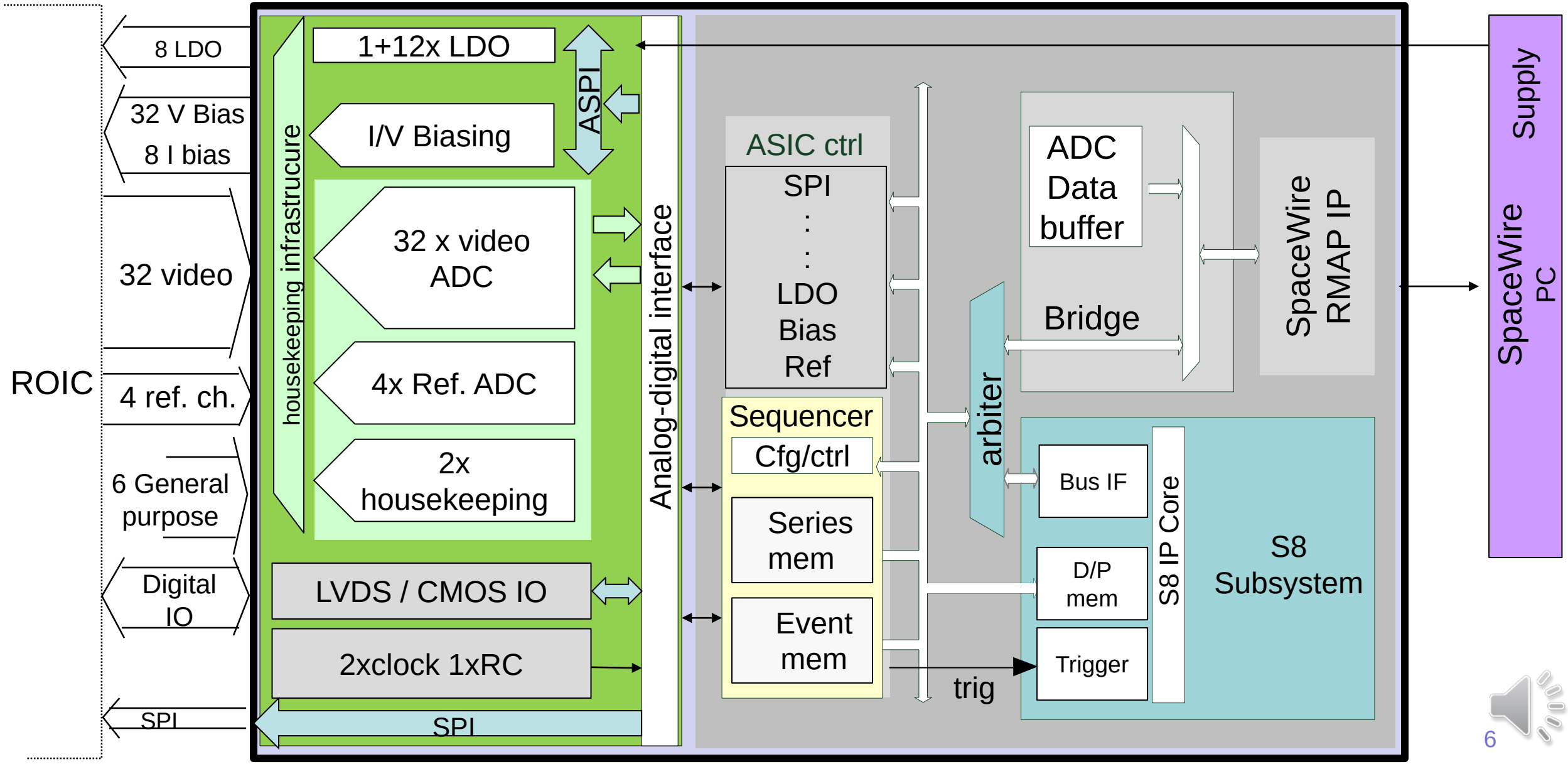
aLFA-C: full chip

- 38 16 bit ADCs
- Digital core: DARE018 Analog core: Caeleste RH
- Technology: UMC018
- Successfully test at RT and Cryogenic:
  - Operational down to 24.5K
  - Characterized at RT, 77K and ~30K
- Performed radiation test
  - TID: up to 290 krad
  - Heavy ion: up to LET 62,5 MeV.cm^2/g

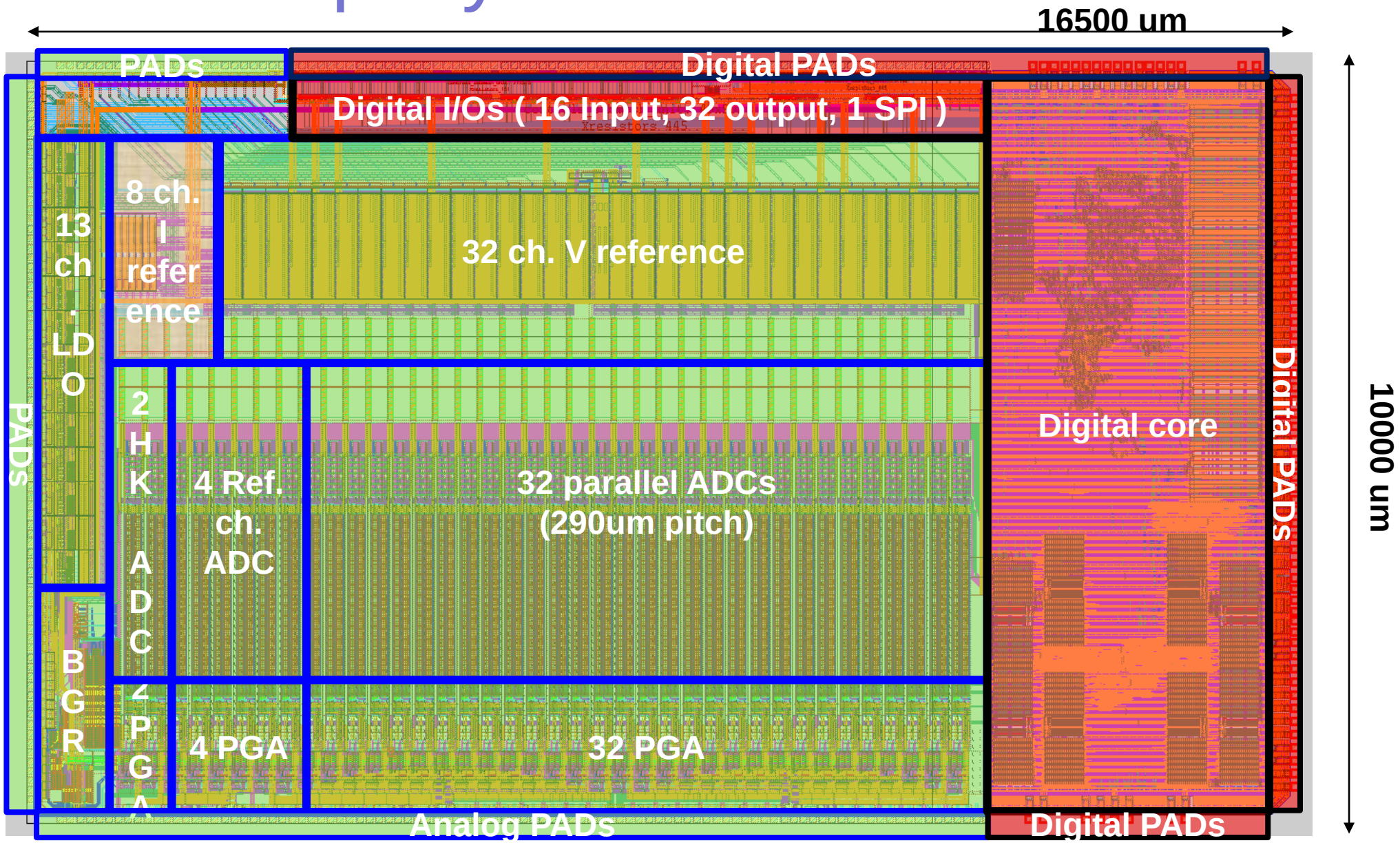




aLFA-C Architecture / block diagram

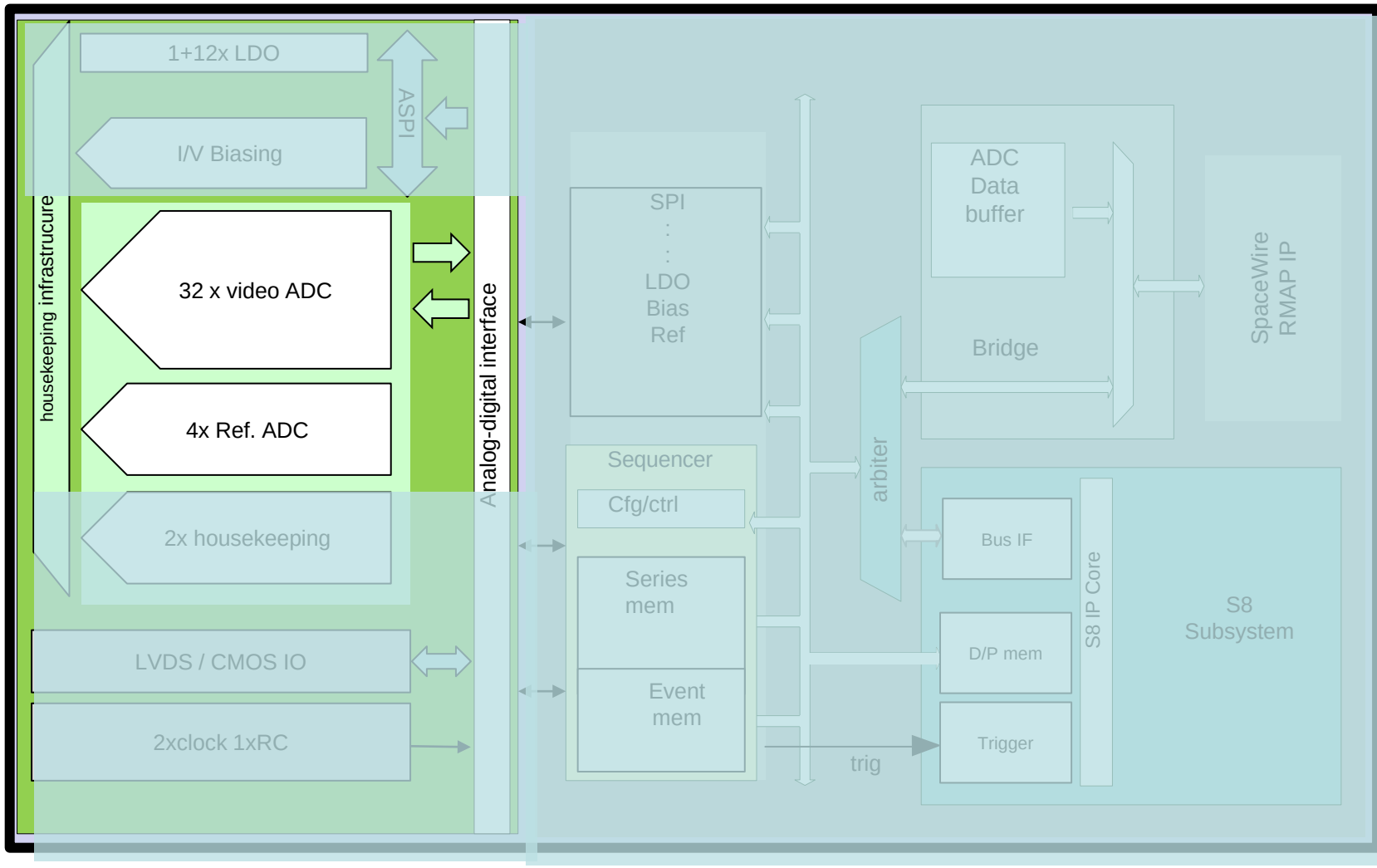


aLFA-C chip layout

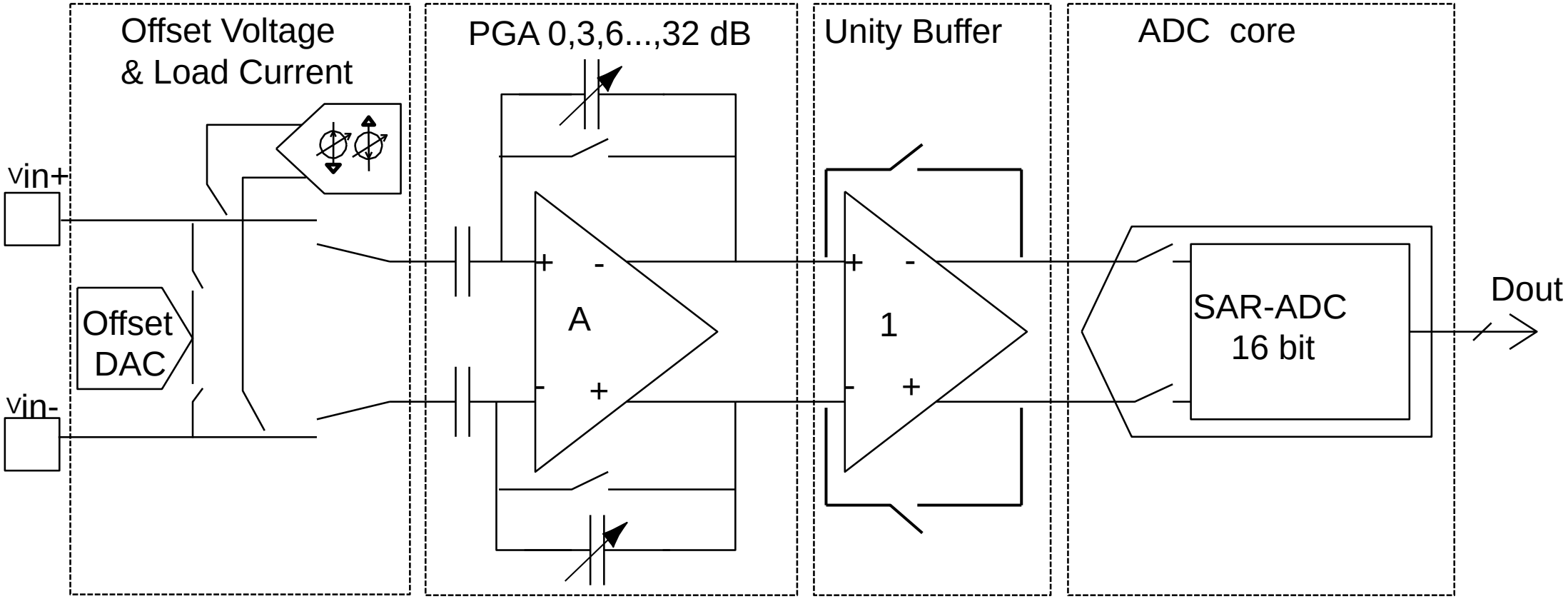


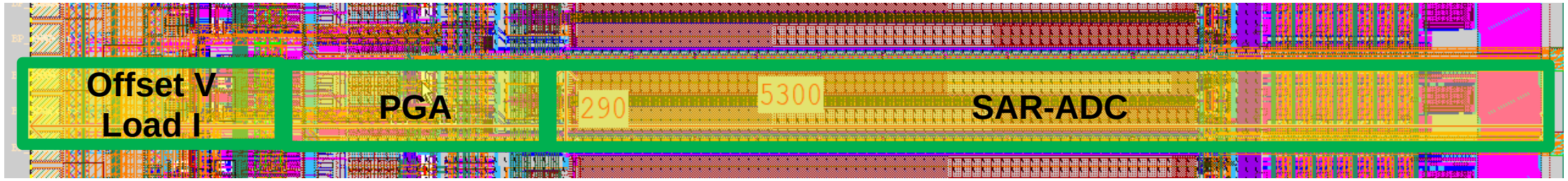
Video channels

- 32+4 channels
- 100ksps
- Input method
  - 32/64 Single ended
  - 32 Fully Differential
  - Parallel or interleaved sampling:
    1/2/4/8/16/32



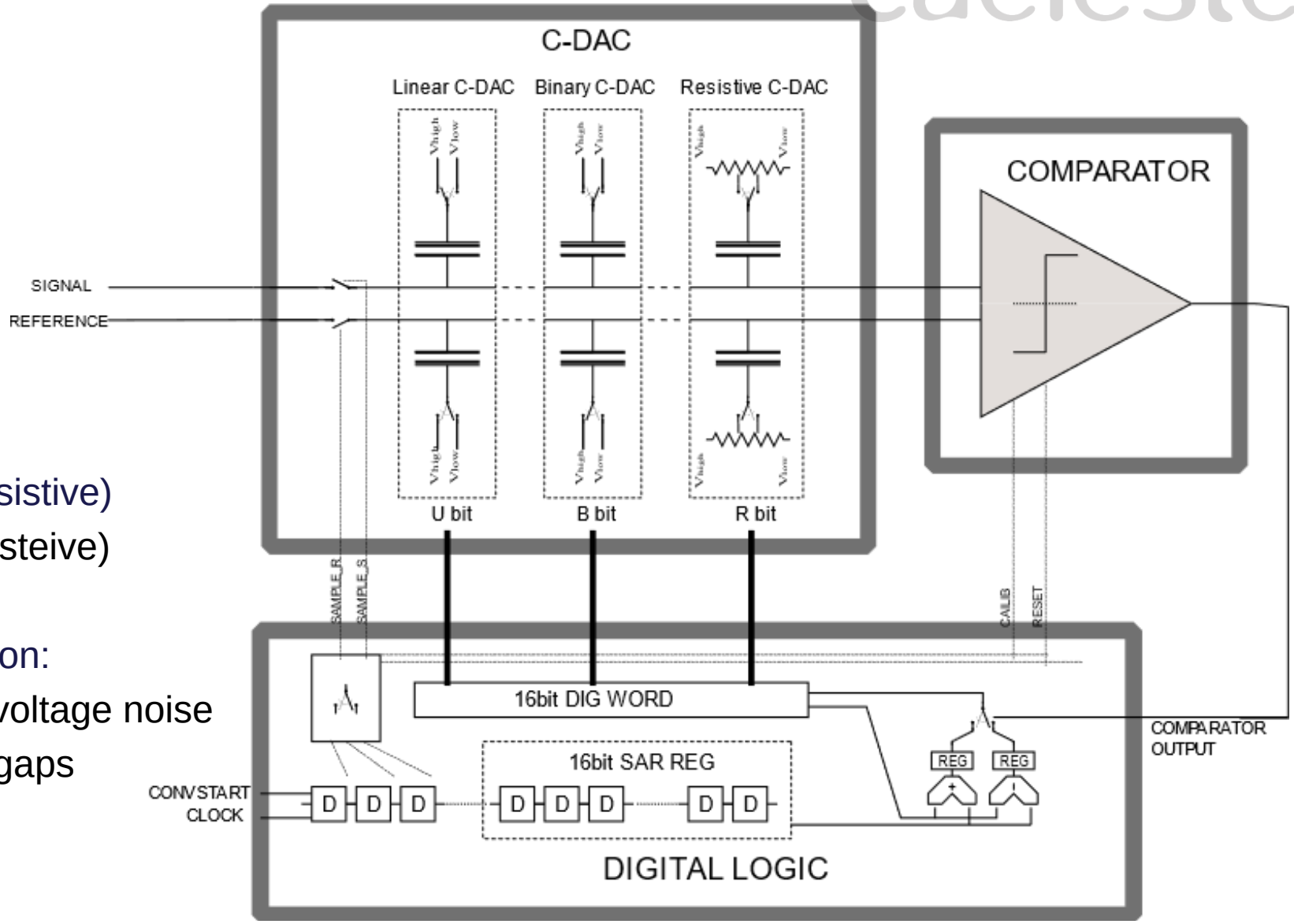
Single “video” channel



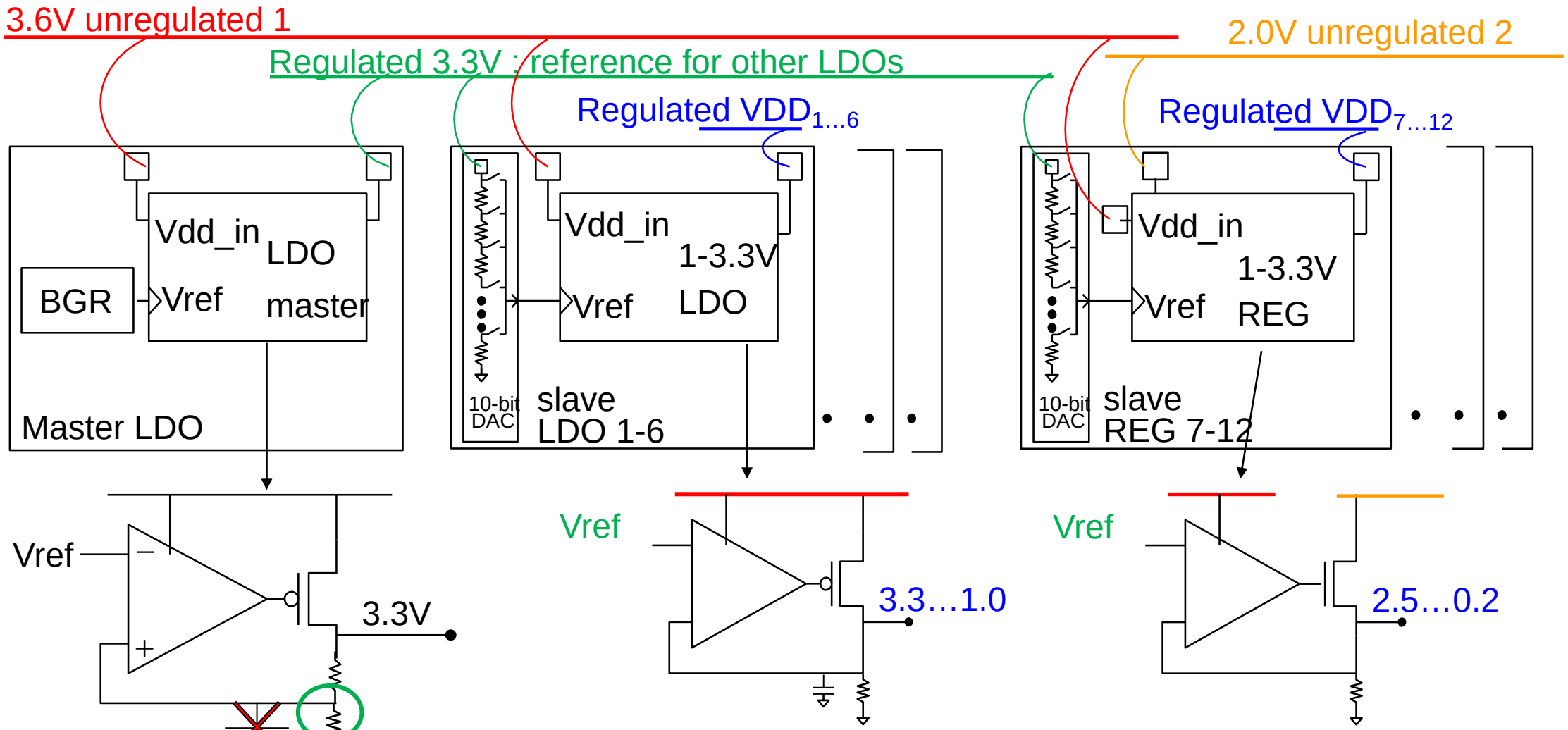


ADC core

- 16 bit SAR-ADC
- 100ksps
- 32 clock for each conversion
- Fully differential
- Upgrade 16-bit SAR ADC
  - C-DAC: 6(unary)+5(binary)+5(resistive)
    - Prototype: 11(binary)+ 5(resisteive)
  - Programmable bit-cycling clock
  - Possible post-conversion correction:
    - Reduce comparator and ref. voltage noise
    - Correct settling related code gaps



Programmable Regulators



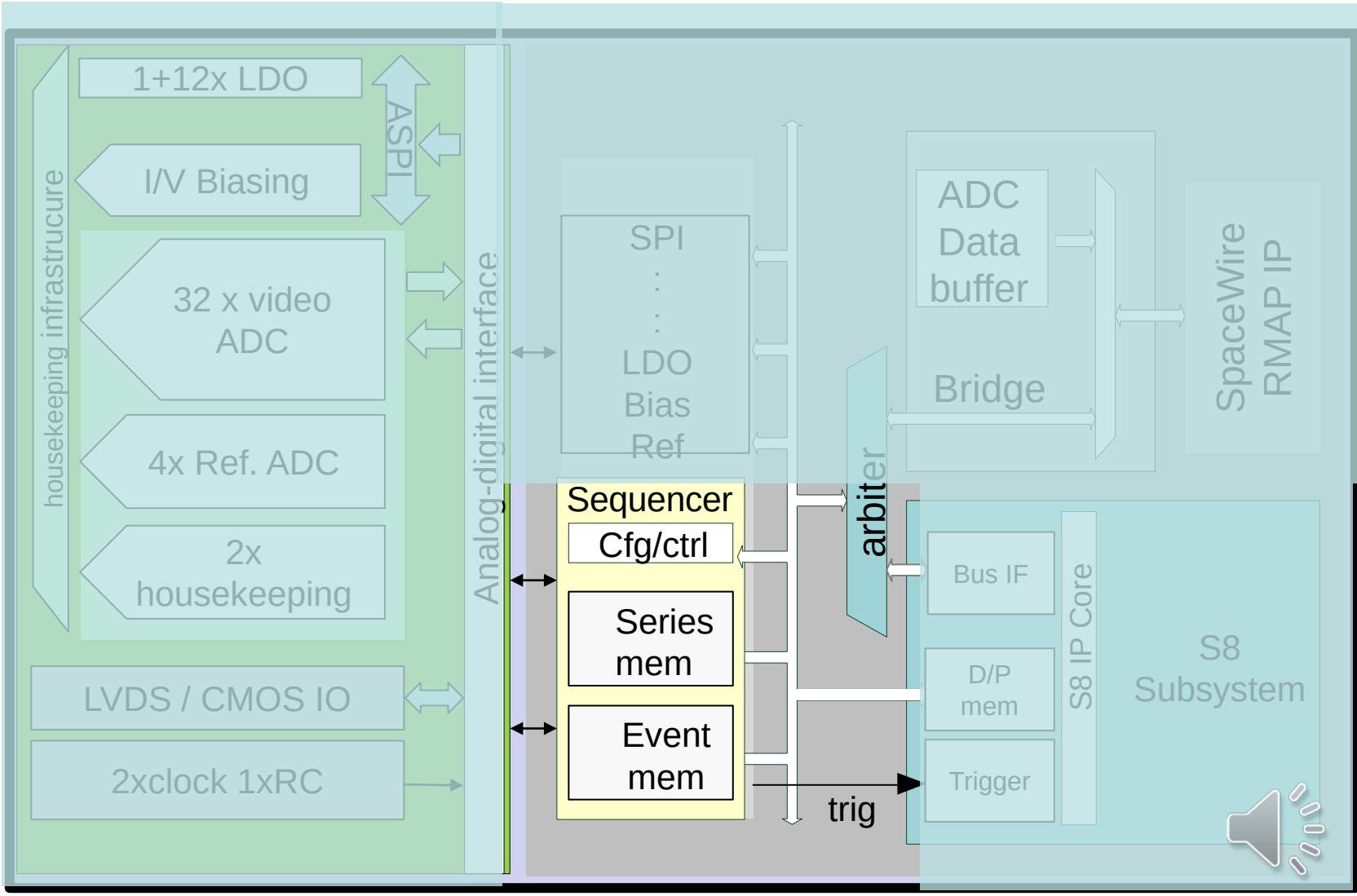
Low programmability
Lesser stability issue

High programmability
Unity gain feedback
Lesser stability issue

High programmability
Regulator with Low drop out
Stable

Programmable sequencer

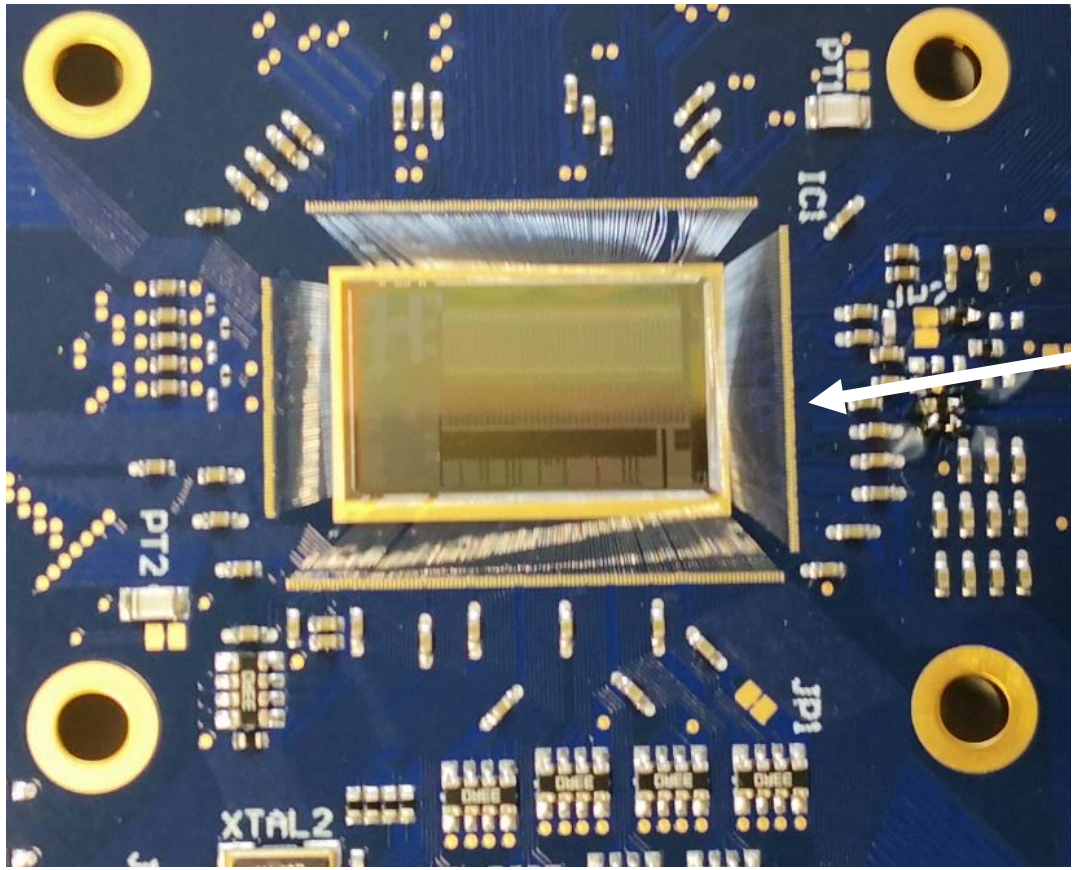
- Control
  - All 38 ADCs
  - All 32 digital outputs
  - All 16 digital input
- Trigger on-chip µ-processer
  - Parameter Sweep
  - Other tasks

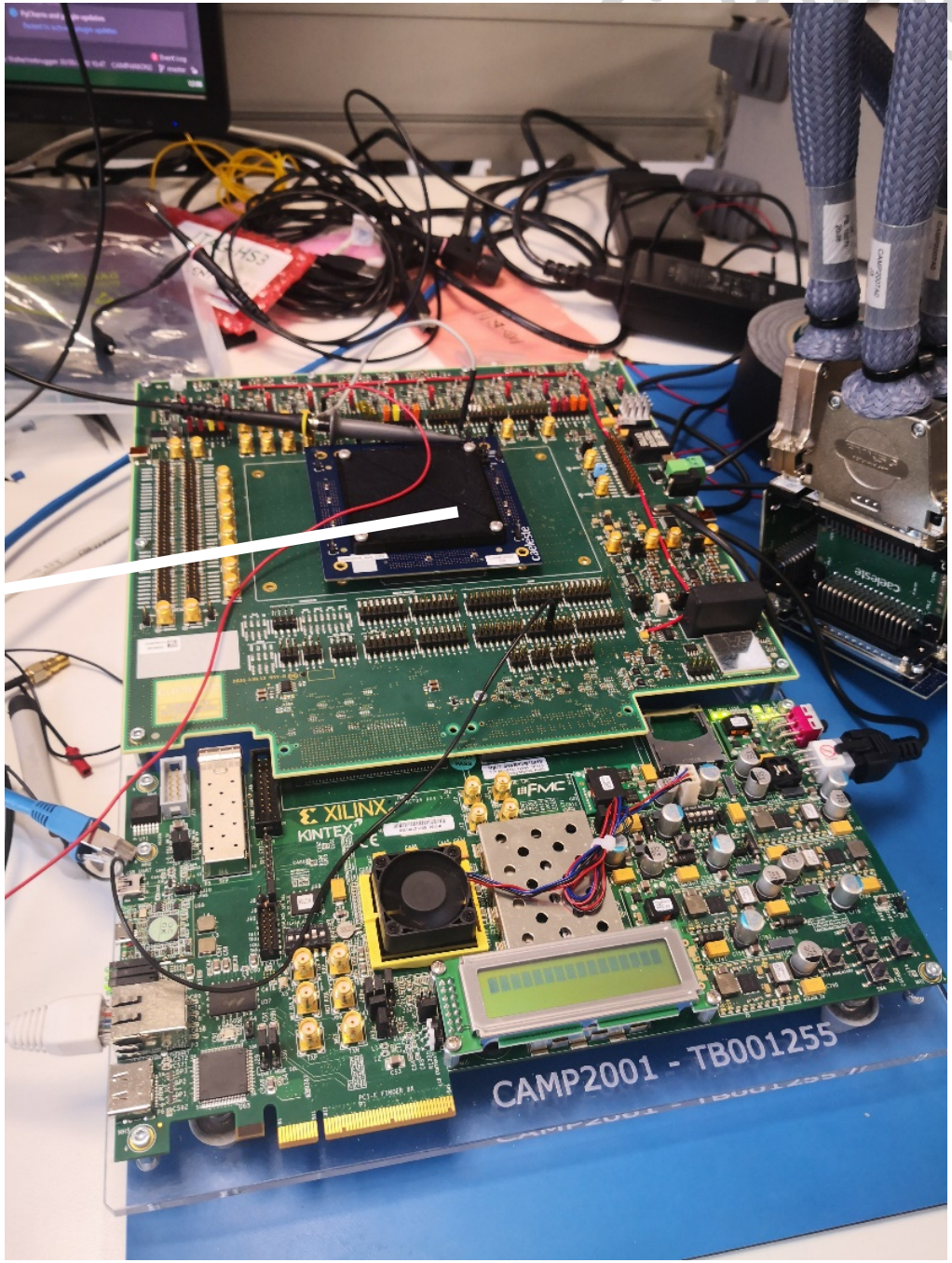


Others building blocks not treated today

- Reference voltages: 10 bit DAC
- ROIC Control I/Os :
  - Logic level programmable
- 4 wire bus for internal/external monitor
  - I/V measurement: LDO,V DAC, T sensor….
  - Video channel auto test…
- SpaceWire & RMAP
- Clock generation
- On-chip µprocessor S8
- …

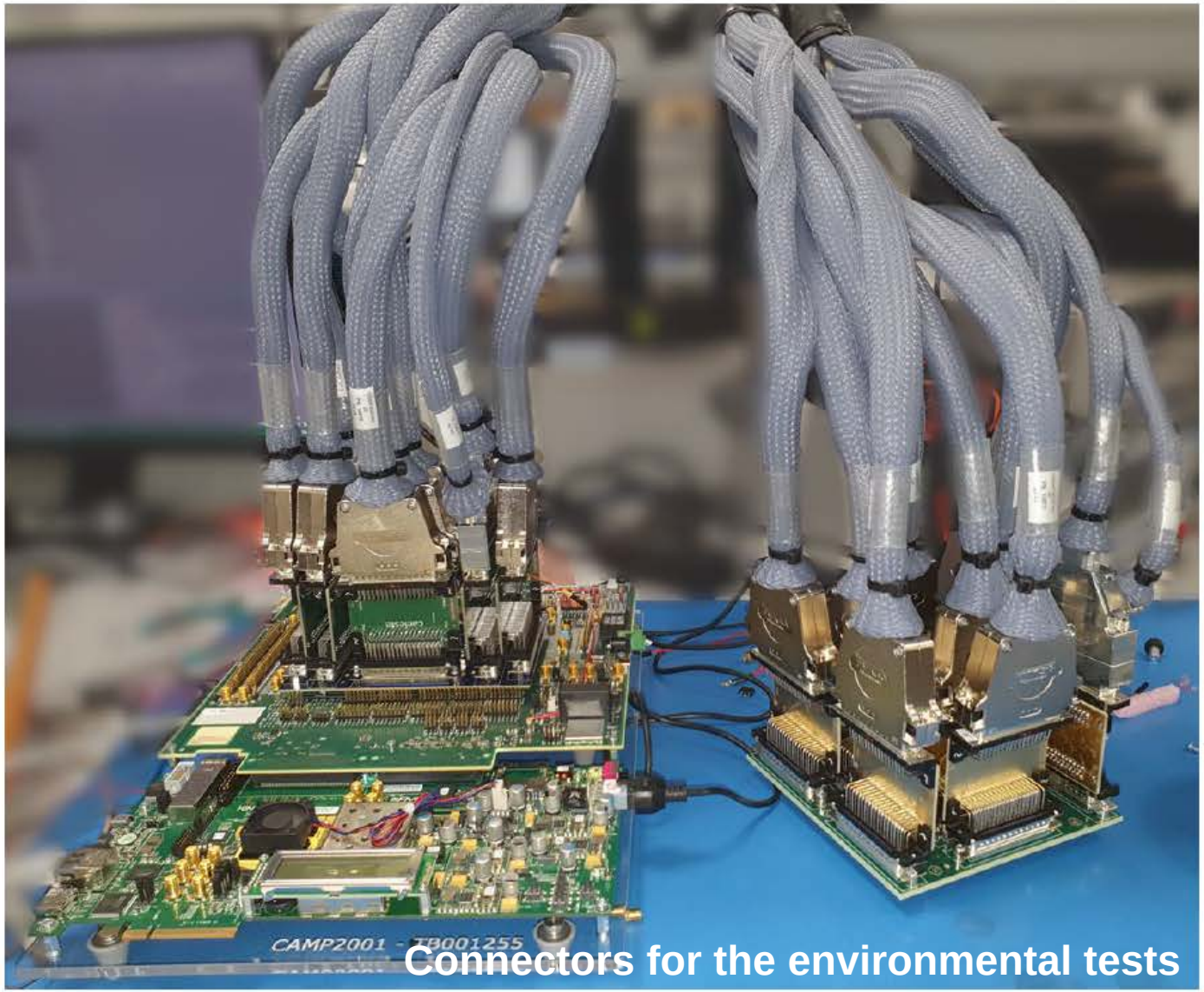
Test setups





RT test at Caeleste

Test setups

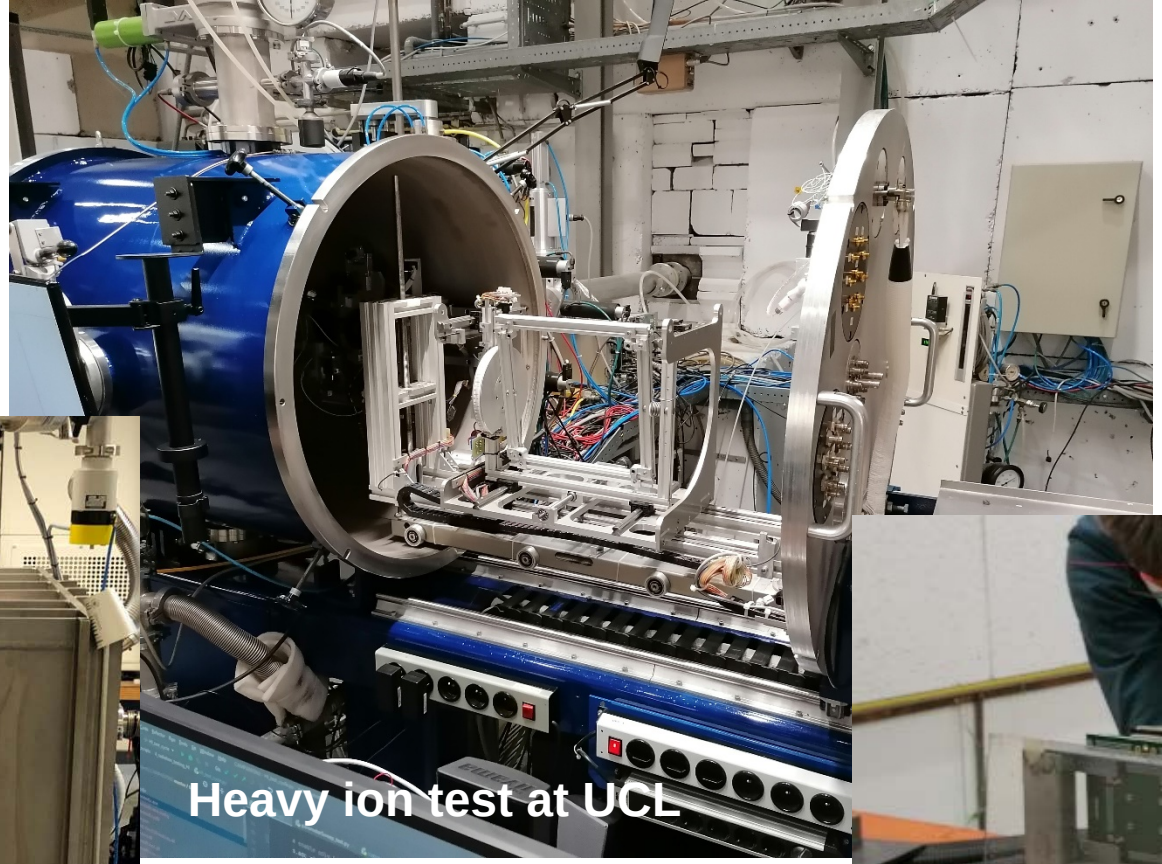


Connectors for the environmental tests

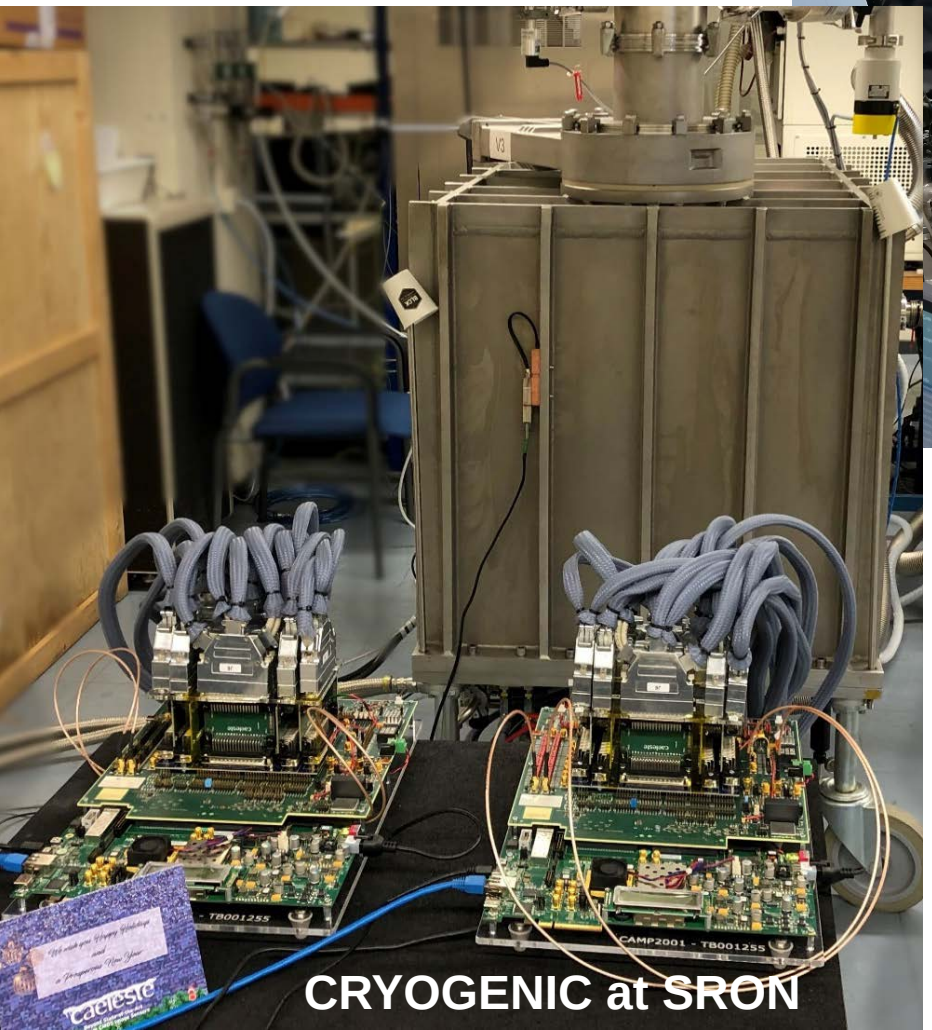
Preparing the environmental tests

Test setups

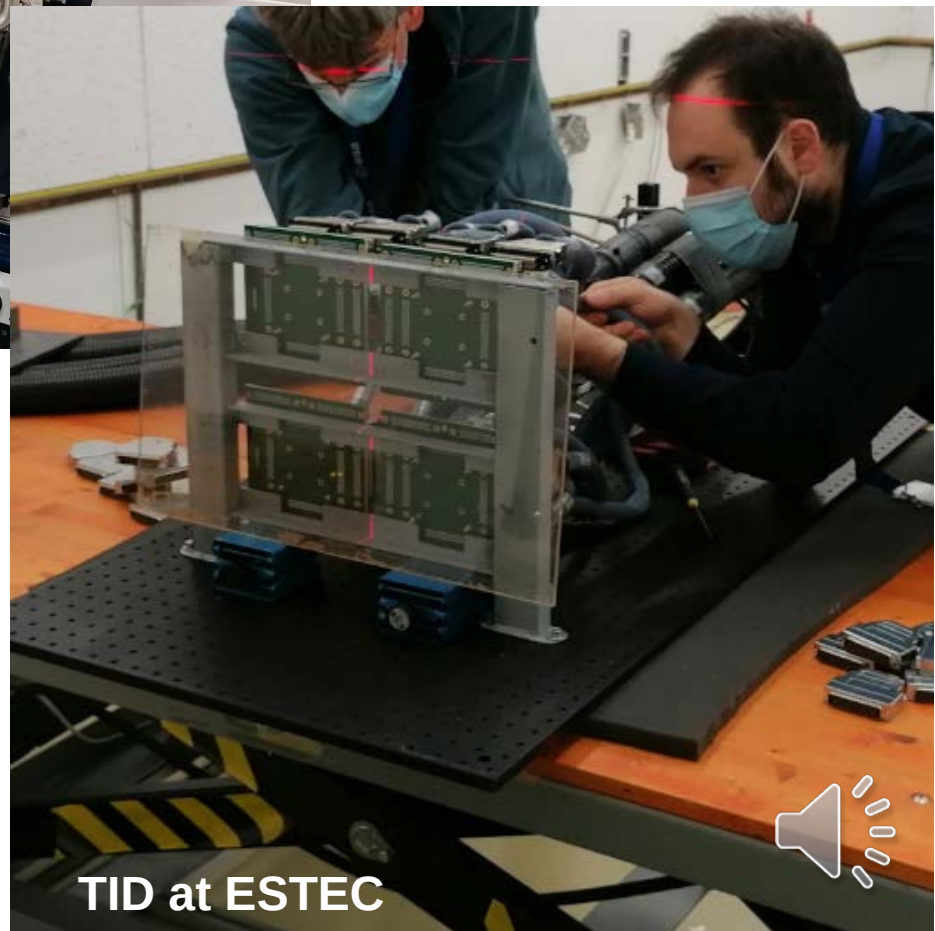
caeleste



Heavy ion test at UCL

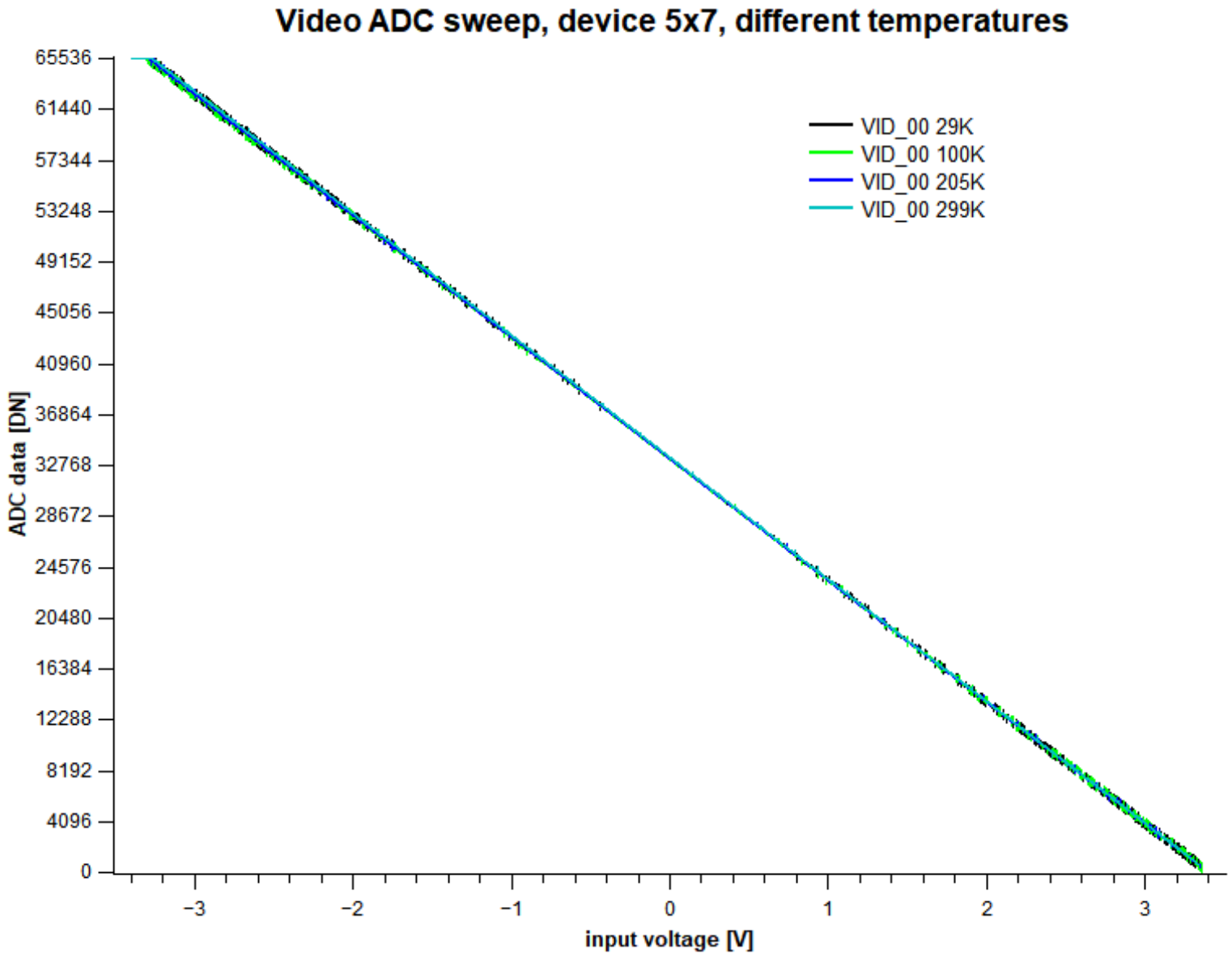


CRYOGENIC at SRON

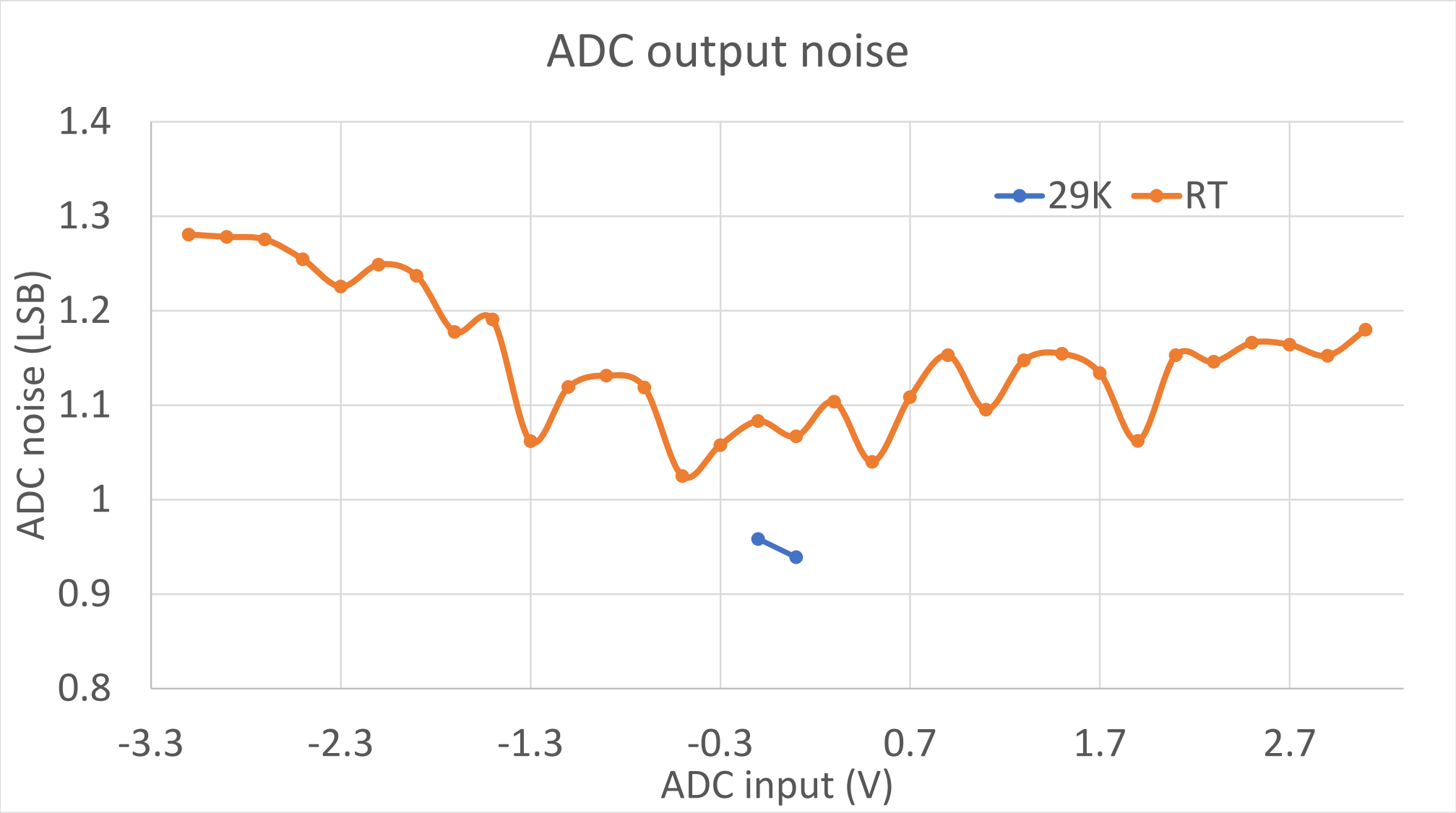


TID at ESTEC

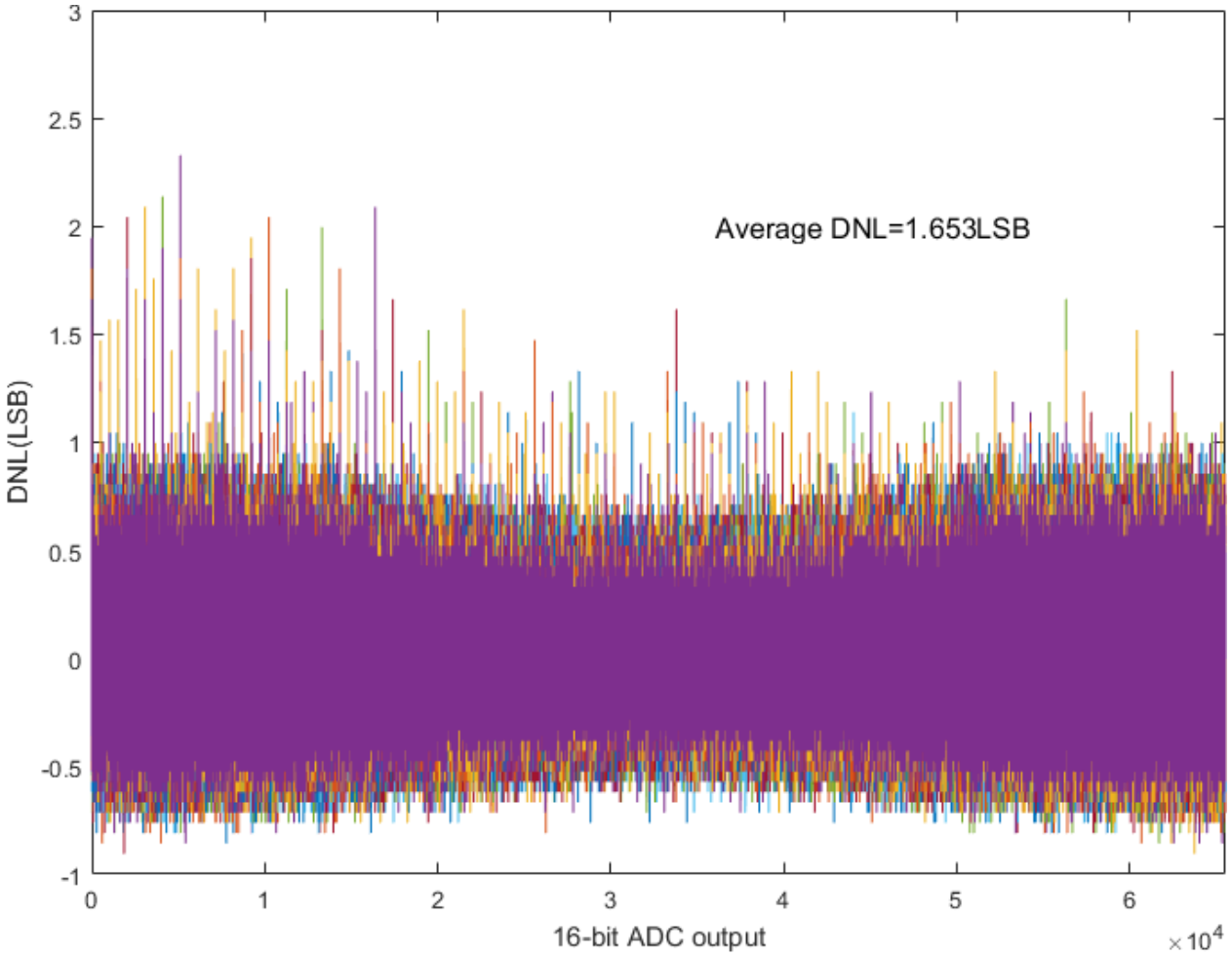
ADC conversion curve

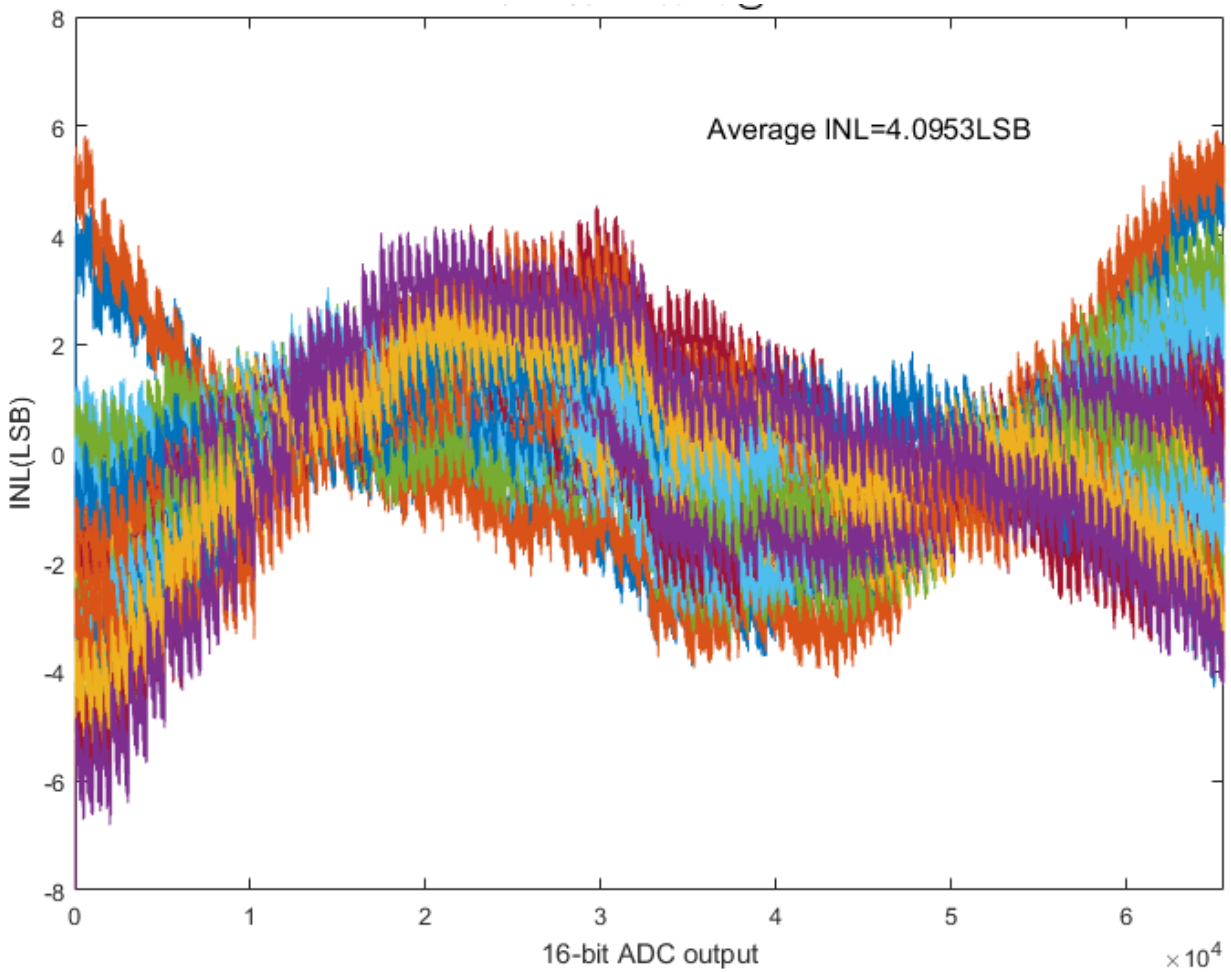


Measured ADC core noise

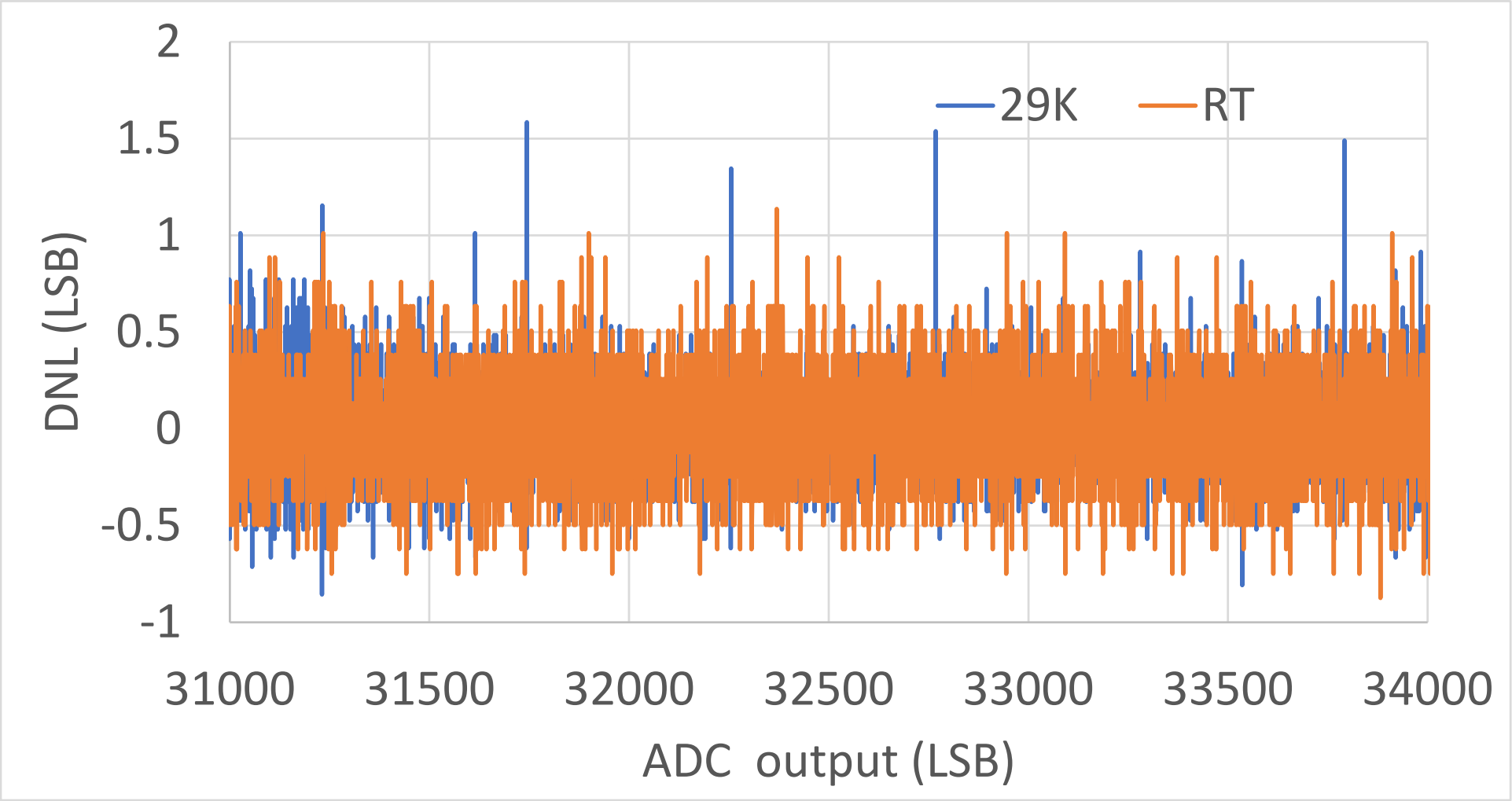


Measurement: ADC linearity @ RT





Measurement: ADC DNL @ 29K



measurement results summary

Specs	Measurement result
Supply voltage	3.5-3.7V (single), 2.0-2.2V(optional)
Regulator PSRR	> 60dB
Regulator I out	> 40mA
Output impedance	< 0,3Ω
LDO output	1-3.4 V
ADC noise	1,15LSB
ADC INL	4,09LSB(average), 6,8LSB(worst)
ADC DNL	1,65LSB (average), 2,65LSB(worst)
Resistance test	4 wire measurement
VDAC output noise	6,8uVrms
Number of digital outputs/ inputs	32 / 16
Digital output clock speed	Up to 20 MHz
Serial interface speed	Up to 20MHz
SpaceWire bit rate	0-200 Mbps
Temperature range	24,5K-room T (Measured)

Conclusions

- aLFA-C ASIC demonstrated all expected features control IR FPAs
  - High solution ADC
  - Lower noise reverence voltage
  - Highly programmable sequence

- Proven operation
  - Room T down to 24.5K
  - Radiation tolerance
    - TID: up to 290krad
    - Heavy ion: up to 62,5 MeV.cm^2/g

Thank you!

For questions or more information, please contact:

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