Radiation hard design in CMOS image sensors

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CPIX Workshop 15-17 sept 2014, Bonn

Outline

- Introduction
- Design for total dose

  ⇒Total ionizon dose TID

  ⇒Displacement damage DD
- Design for single events

  ⇒SEU single event upset

  ⇒SEL single event latch-up
- Take home message

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Introduction

About us

Background in Radhard CMOS design

About us

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Founded 2006

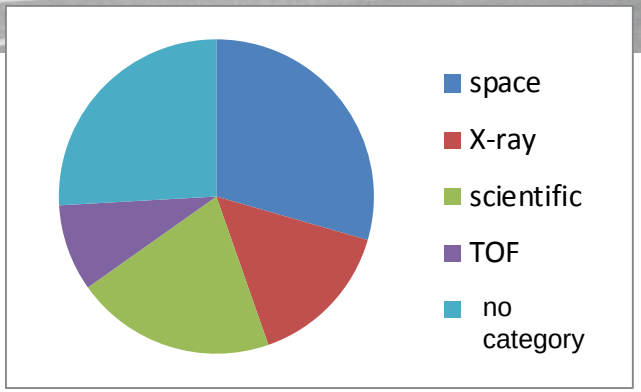
Mechelen, Belgium

17p

Mission

and business model

- Supplier of
- Custom designed
- Beyond “State of the Art”
- Image sensors



Caeleste radhard background

Where we come from

- ⇒Historical contribution to radhard and cryo design for space (ISOPHOT..., OISL, STAR250, HAS...)
- ⇒Background in design for particle physics and X-ray integrating and photon counting detectors
- ⇒Close relationships with foundry technologists
- ⇒Expertise in circuit & device physics & technology

Present

- ⇒Routine radhard design (TID, TnID, SE, SEL)
- ⇒Proton & SE hard pixels
- ⇒ROICs and image sensors

Heritage

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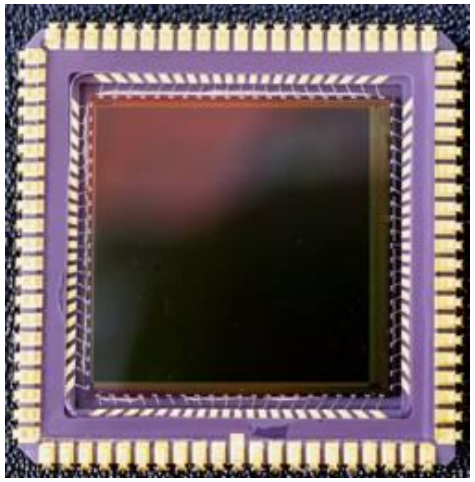
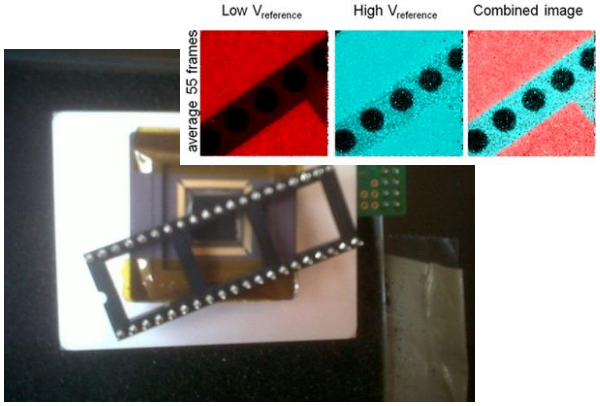
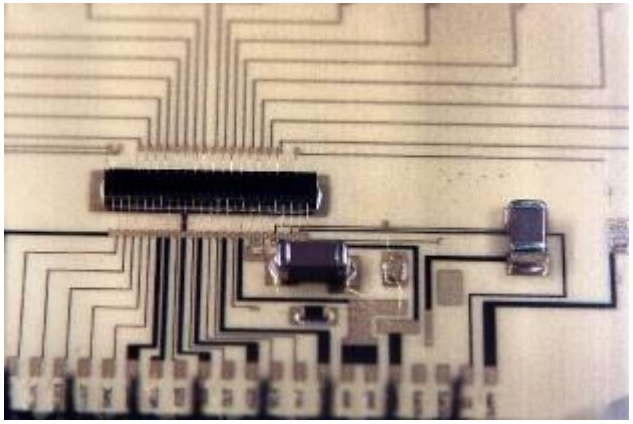


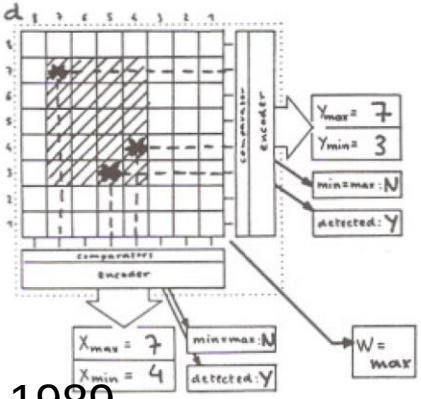
OISL 2000
first >10Mrad



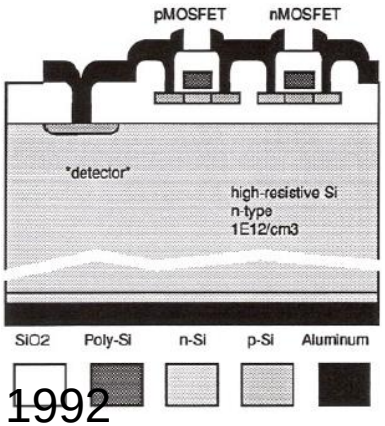
QX 2010
Analog domain 2-energy "color" X-ray photon counting



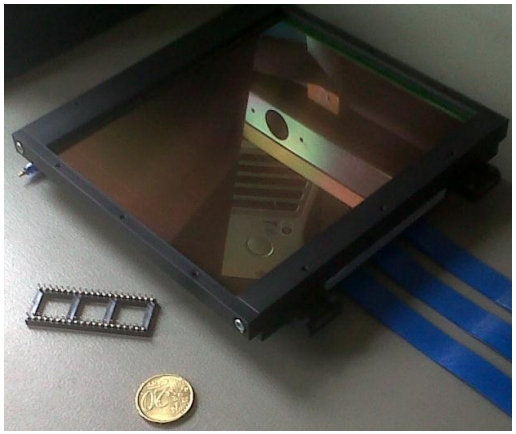
ISOPHOT FIR ROIC 1989
SEU hard wo TR



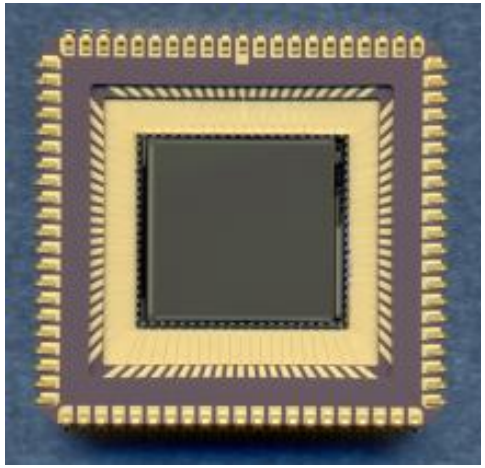
1989
XYW event detector



1992
RD-19 SOI-CMOS



2013 wafer scale X-ray



STAR250/1000 2003

Disclaimer

- This paper focuses on design countermeasures, while understanding the damage mechanism itself
- This is not a design course. Details of actual designs are not shown
- Technology countermeasures, temperature effects, annealing not treated
- No guarantee on effectiveness of techniques, nor of IP freedom

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TID
total ionizing dose
also referred to as IEL ionizing energy loss

TID

Radiation:

⇒Primarily X, γ, but essentially all particles

Dominant effect :

⇒Creation of positive space charge in the SiO2 (SiN) dielectric layers

⇒Also: increase of interface states at Si-SiO2 interface

Effect on CMOS circuits:

⇒ Moderate shift of Vth, μ degradation and 1/f noise increase

⇒ Parasitic S-D leakage via STI/field in nMOSFETs resulting in large dissipation and malfunction

TID

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Effect on CMOS pixels:

- ⇒ Moderate offset shift and 1/f noise increase
- ⇒ Lateral shunting between pixels
- ⇒ Lower gain and increased PRNU
- ⇒ Increased average I_{dark} and DNSU

Most publications are describing this last effect

Design countermeasures

- Buried diodes as the general way to reduce dark current
- Avoiding the parasitic source-drain leakage in nMOSFETs
- Several case-by-case other measures

TID-hard CMOS

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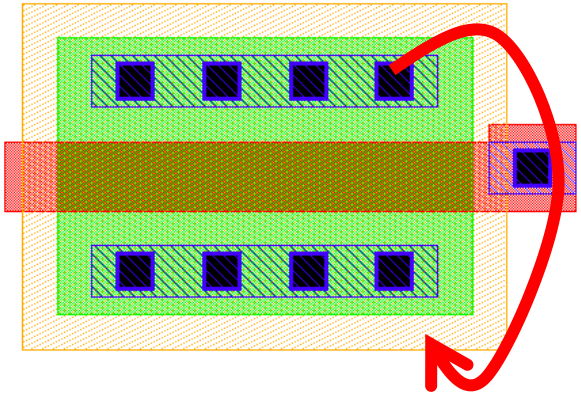
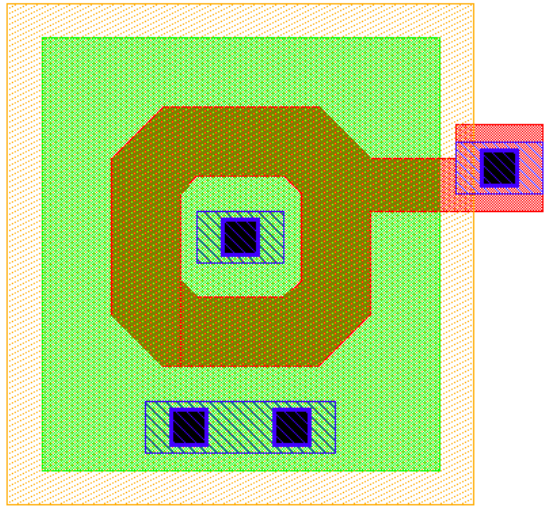
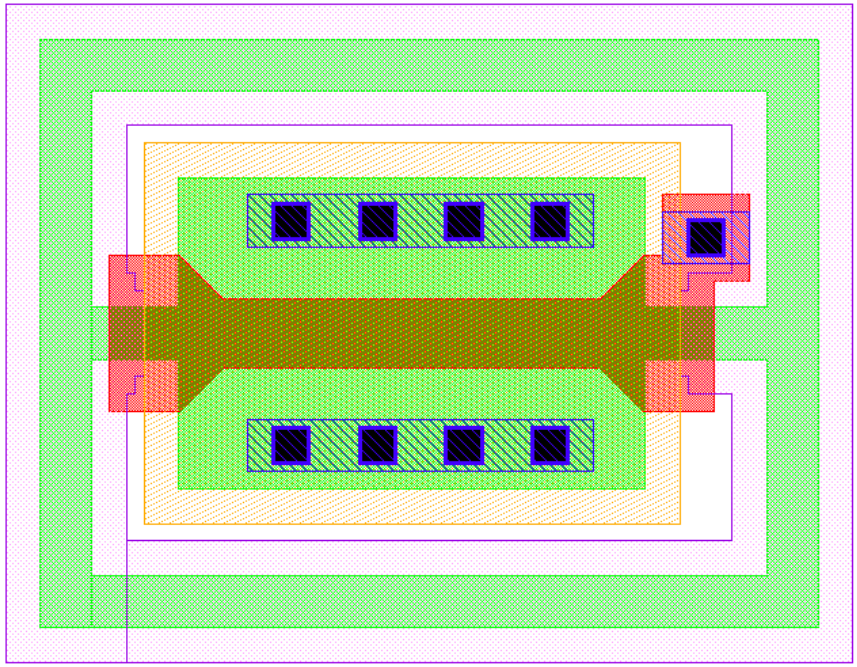


Regular transistor

Leaks when STI/field inverts

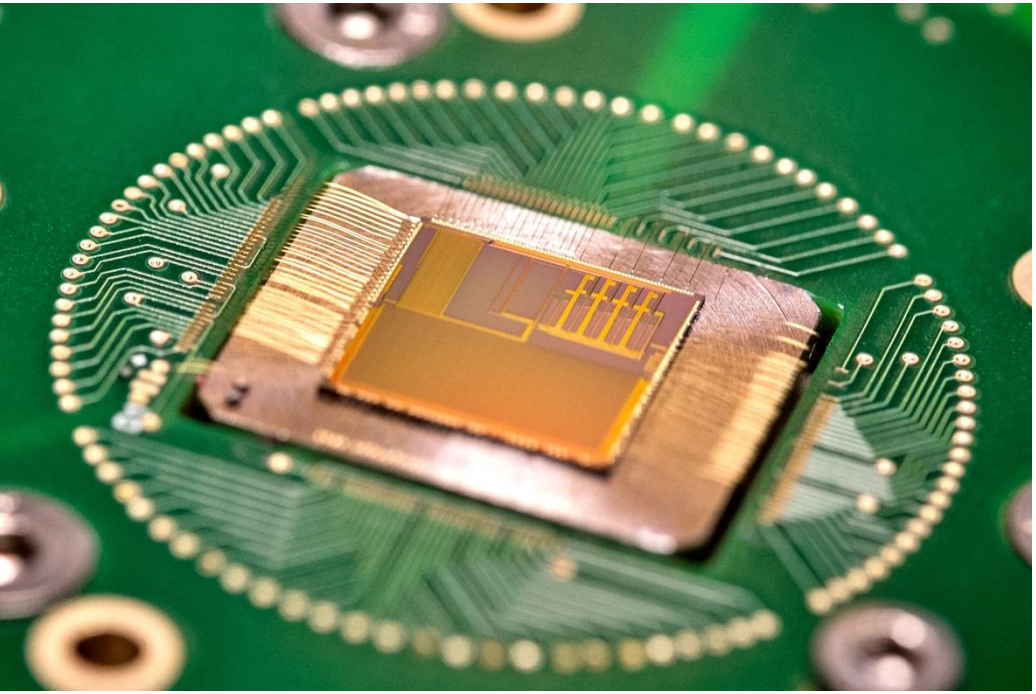


Annular transistor:
No path over STI/field



H-gate transistor:
Leakage path over STI/field is blocked by P-implant

The “CES” IR ROIC



Fully radhard & cryo$_{77K}$

UMC018

Digital: DARE library

Analog: CaelesteRH

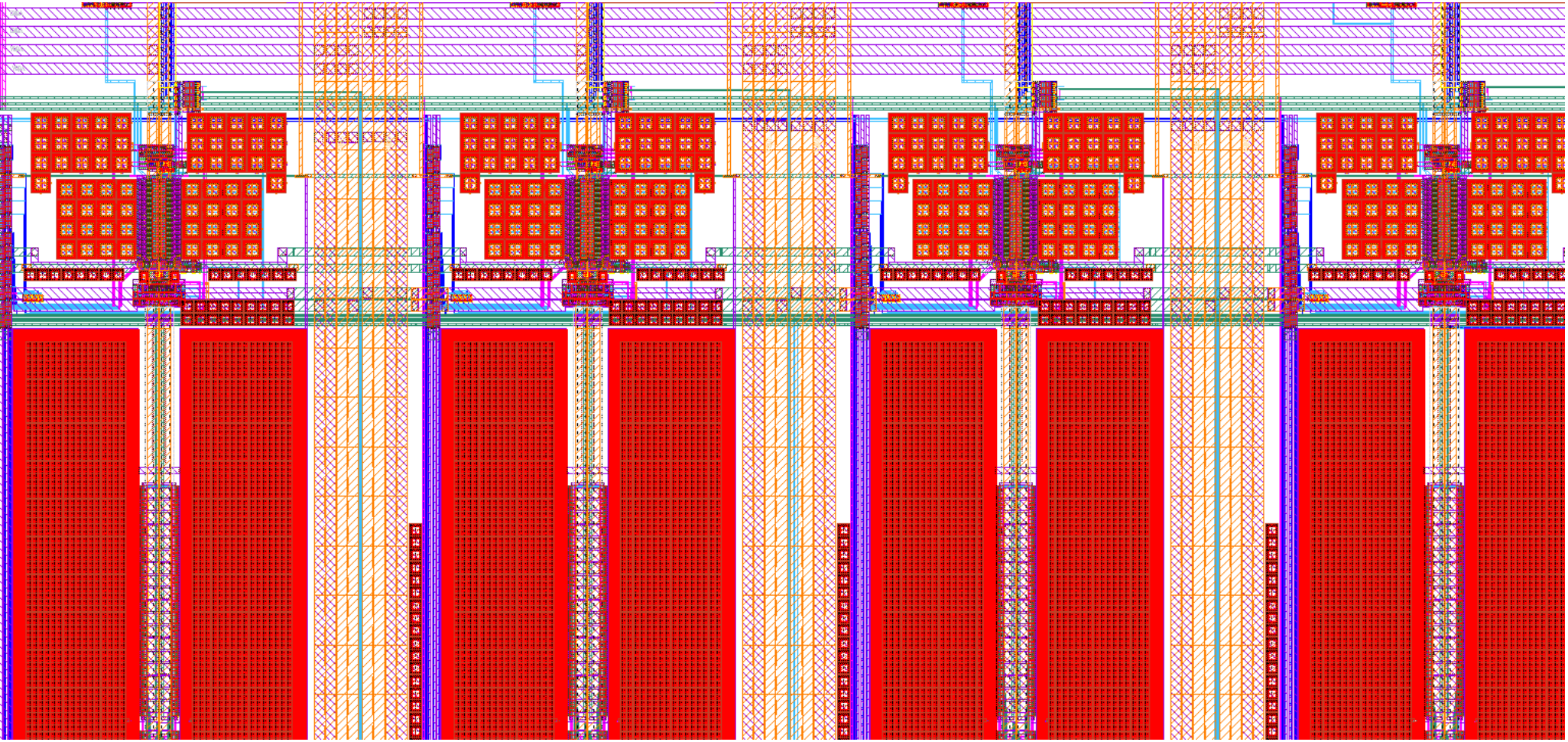
>>1Mrad, not tested yet

ESA consortium

Caeleste+Easics+Selex

2014

4 SAR ADCs, detail



Digital logic, detail

Caeleste RH library

CaelesteRH as compared to SotA

Available in 3 technologies, porting is standardized

Full analog & mixed mode

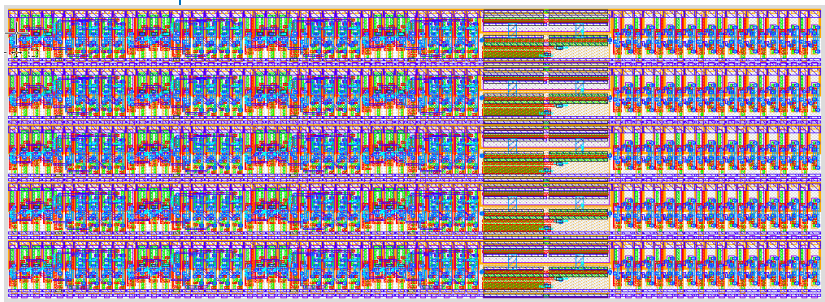
Very high TID & TnID hardness

Very high SEL hardness

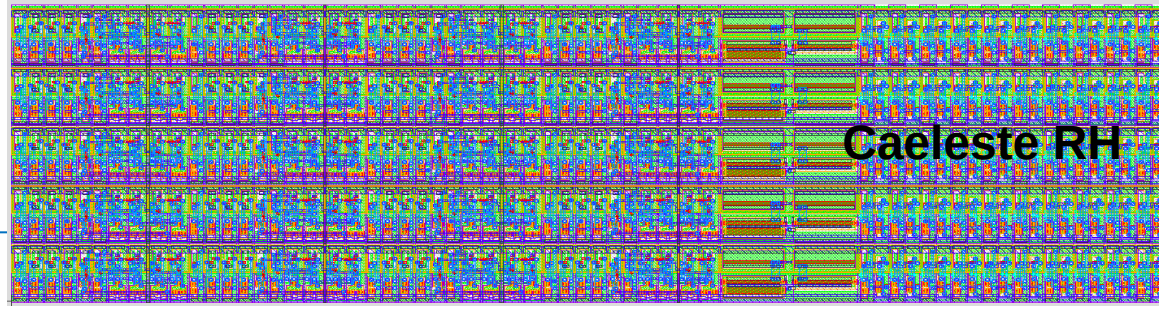
Very high SEU hardness wo TR

<20% increased Cin and power

<50% area increase



Normal Caeleste mixed mode



Caeleste RH

TID Gamma Radhard pixels

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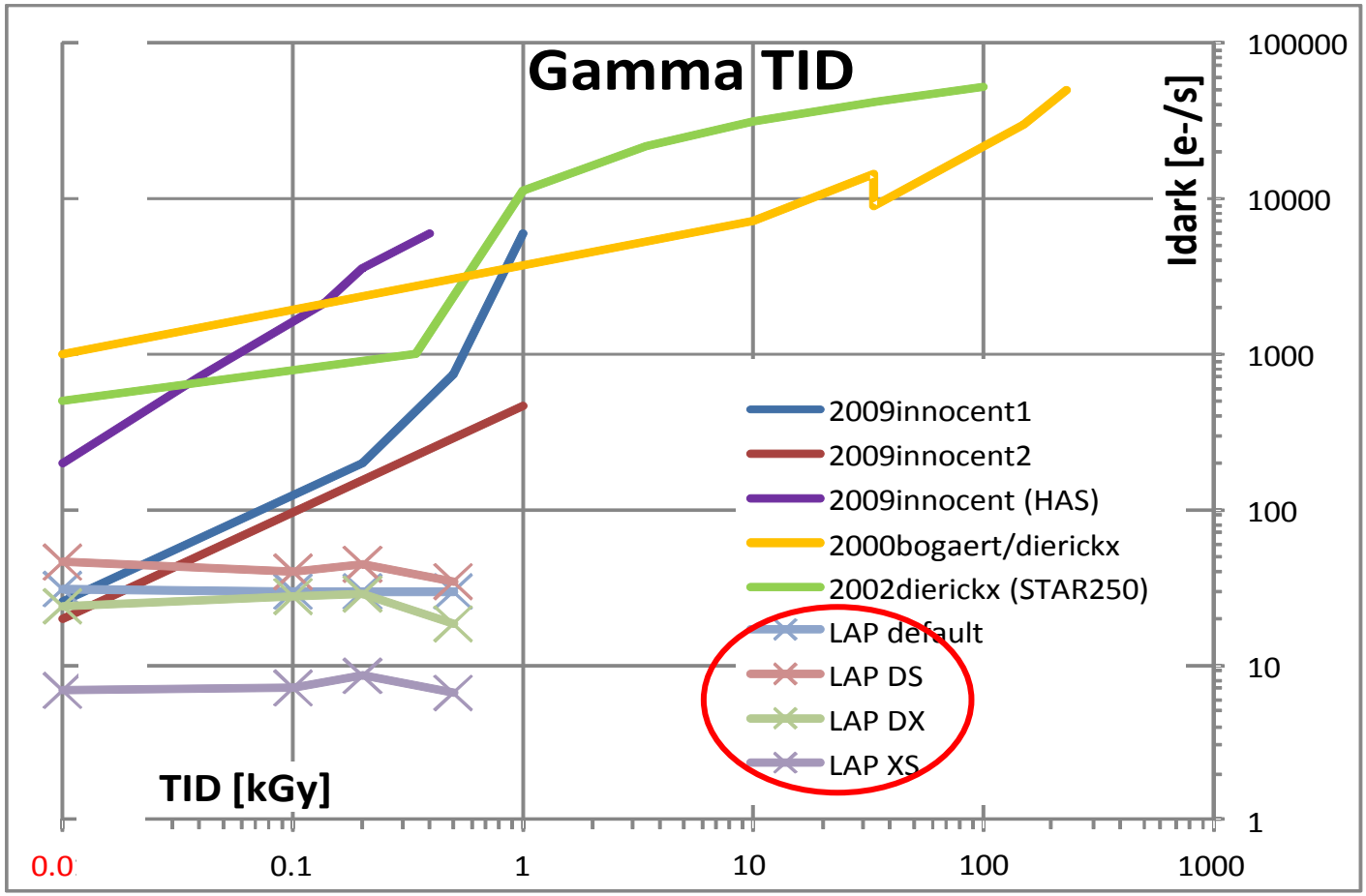
LAP2010 device

Tower TSL018

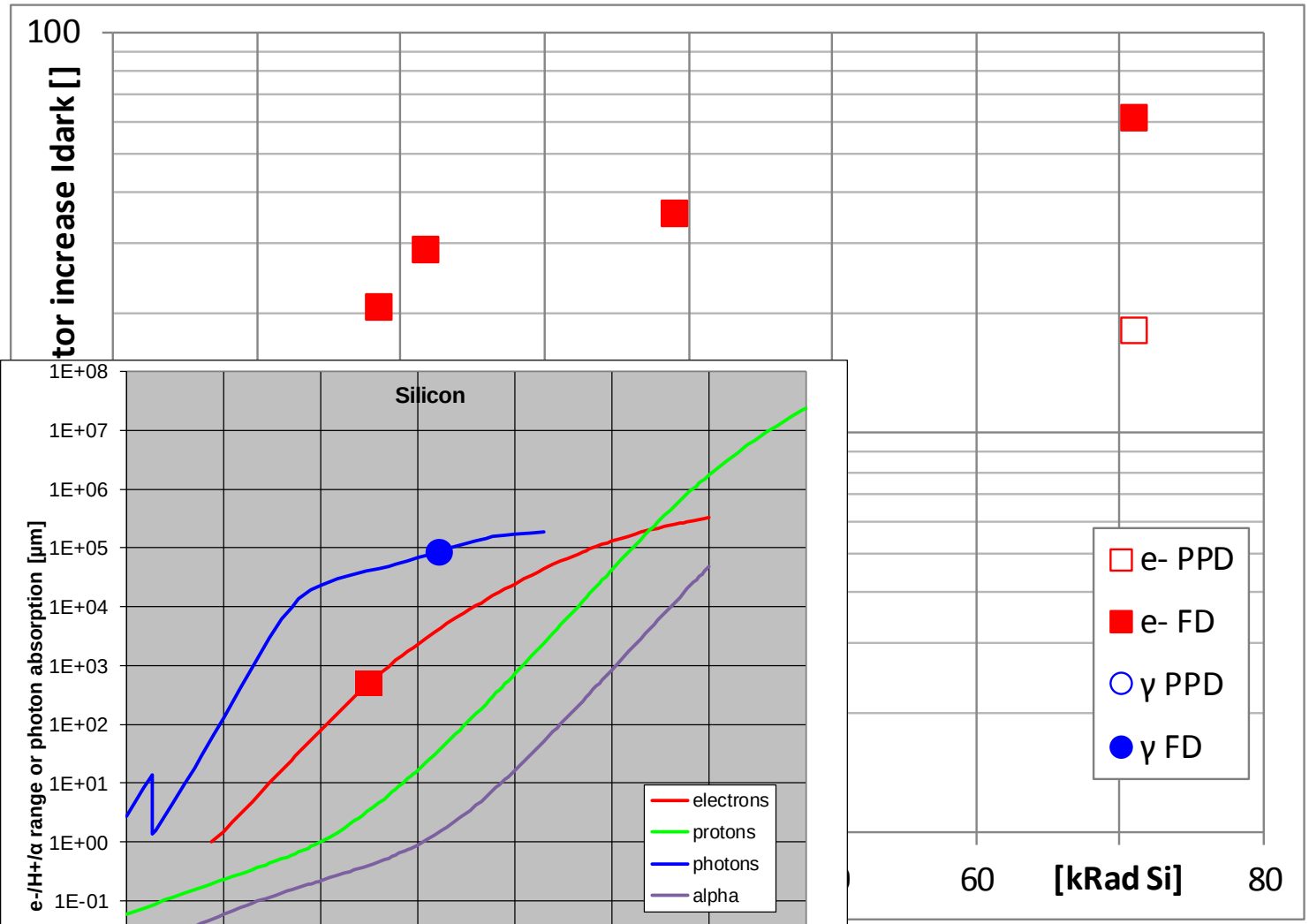
2011

TID of gamma ^{60}Co

Compared to published SotA



TID Gamma ≠ Electrons



LAP2010 device

Tower TSL018

10 devices; many pixels per device

TID of

- 300keV electrons
- 1.2/1.3 MeV gamma ^{60}Co

Effect on

- Buried PPD
- Surface FD

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DD displacement damage

also referred to as “NIEL”
non-ionizing energy loss

DD

Radiation:

⇒HE particles: protons and heavier

Dominant effect :

⇒Non-elastic displacement of Si atoms

⇒Often creating an initial vacancy+interstitial

Effect on CMOS pixels:

⇒ Point-wise heavily leaking diodes, hot pixels

⇒ Often blinking “RTS” dark current pixels

Photodiode redundancy?

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Proton/Neutron/other_particle

⇒ displacement damage in the photodiode creates “hot” or “RTS” pixel

⇒SE creates flash

No way to remove or calibrate this?

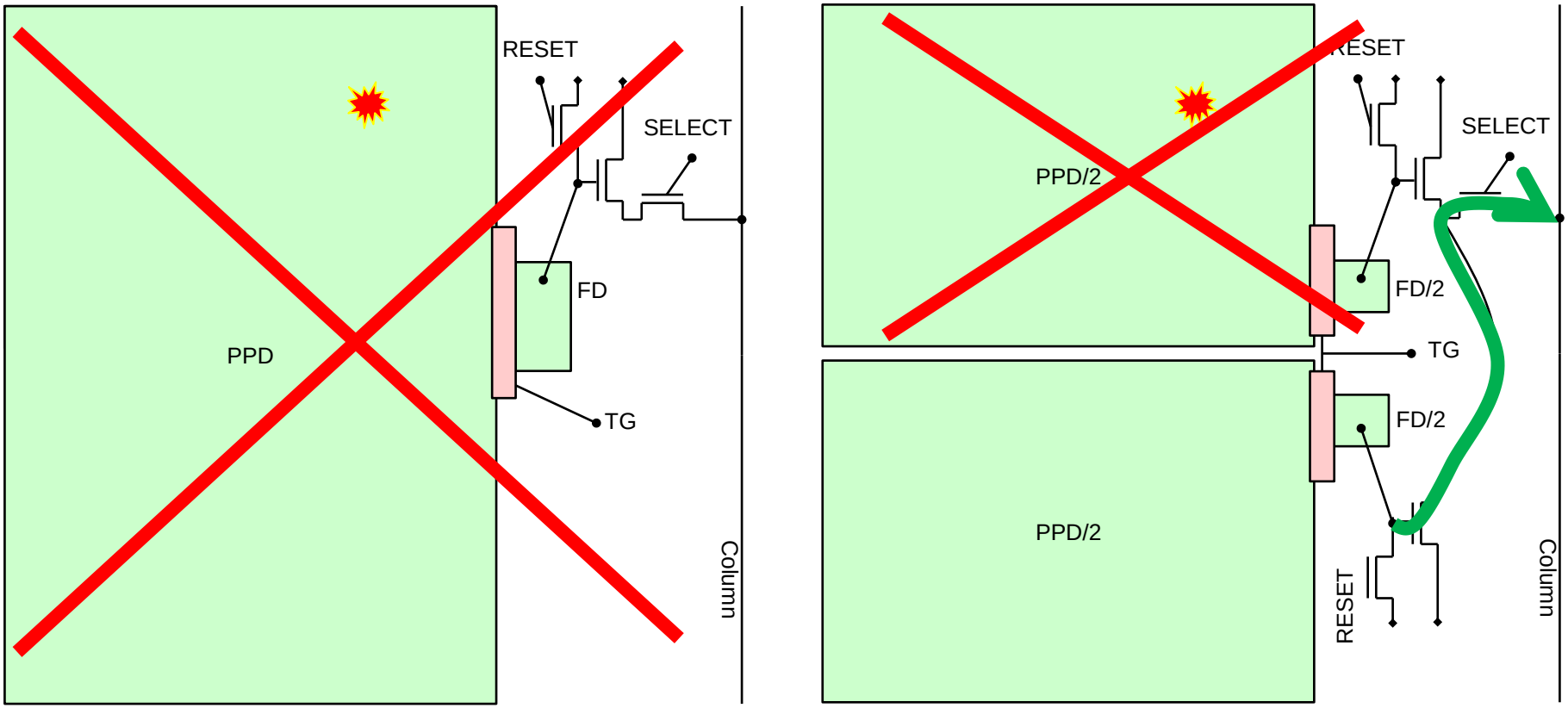
Suppose we split the pixel in 2...100 parts. The defect will reside in only one

Redundancy?

⇒Readout all, remove the defect part’s signal and average.

⇒Take a weighted maximum voltage by winner take all circuit or sourcefollower

Photodiode redundancy



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Introduction
TID total ionizing dose
DD displacement damage
SEU single event [upset...]
SEL single event latch-up
Take home message

SEU

single event [upset]

Also SEE, SEFI, SET, SEGR, SEB ... ()

SEL is separately treated

SEU

Radiation

⇒Sometimes X, γ, e-, but rather much heavier particles

Dominant effect :

⇒Creation of instantanous + or – charge packet sufficient to toggle a latch

Effect on CMOS and CMOS pixels:

⇒ register or memory loosing information

⇒ flash seen by the photodiode

SEU

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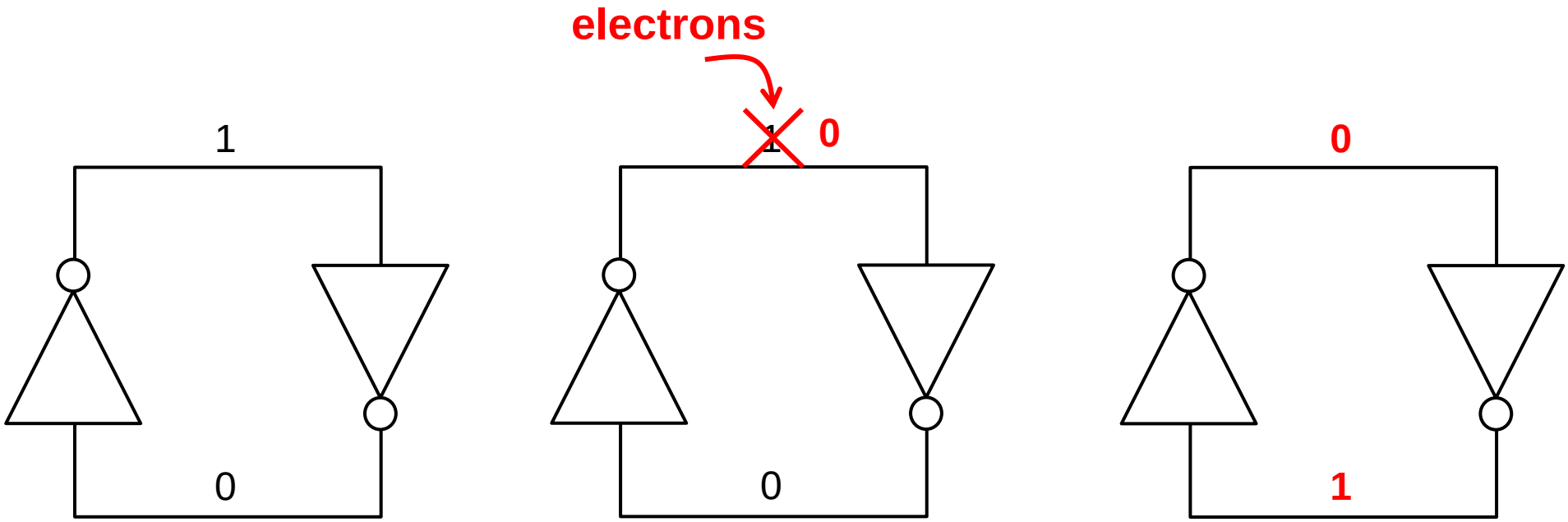
⇒The loss of bits in SRAM cells or Flip-flops



SEU

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Mechanism

- Particle deposited charge packet charges one node of a latch to the oppisite logic value

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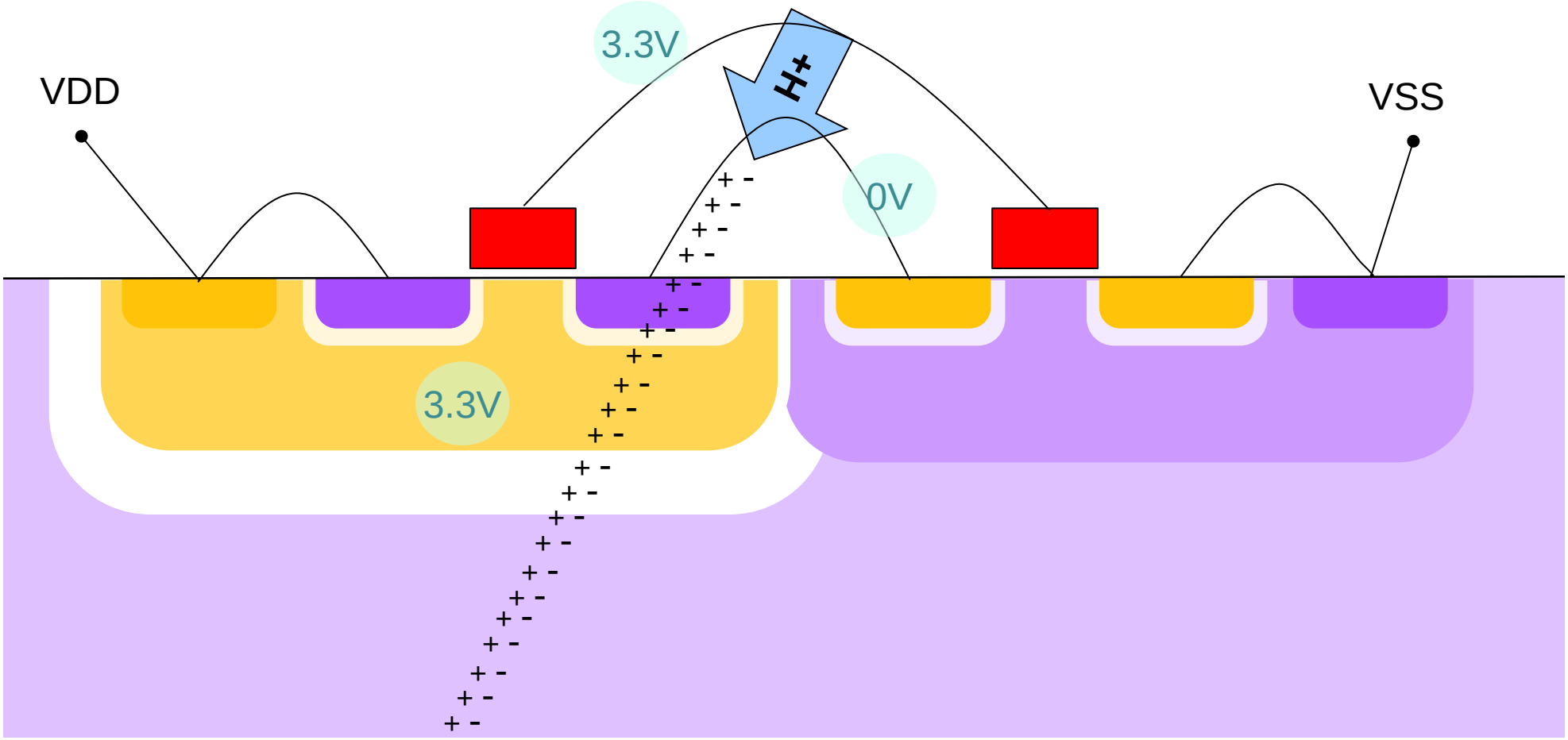
Flipping the invertor @t_0



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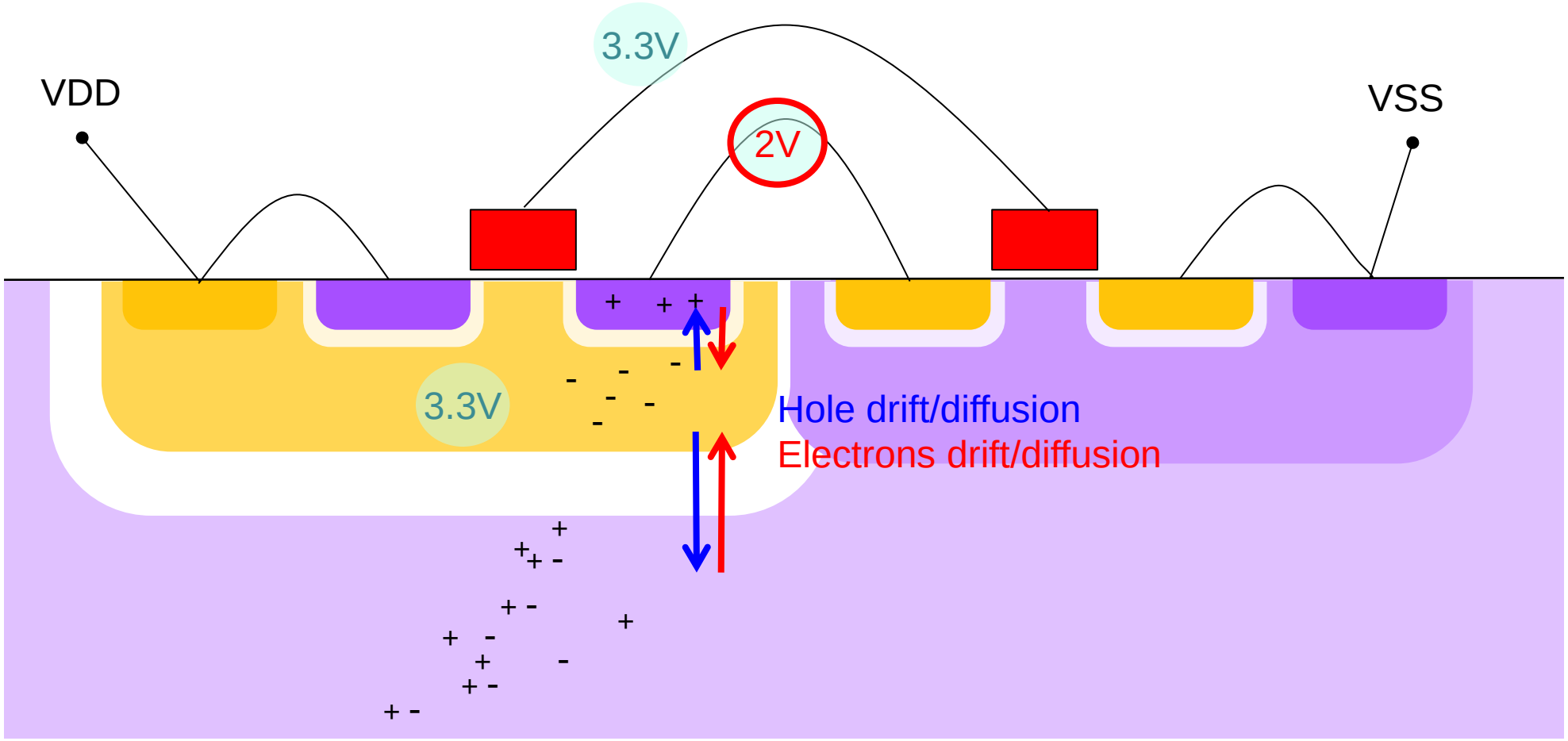
Flipping the invertor @t_0+0.5ns



SEU countermeasures

- Shield against particles
- Make vulnerable volume small
- Make vulnerable node capacitance large
- Triple (and other froms of) redundancy
- Detectability, read-back, re-upload

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Introduction
TID total ionizing dose
DD displacement damage
SEU single event [upset...]
SEL single event latch-up
Take home message

SEL

single event latch-up

SEL

SEL

Radiation

⇒Protons and rather even heavier particles

Dominant effect :

⇒Creation of instantanous + or – charge packet sufficient to initiate a PNPN latch-up

Effect on CMOS:

⇒ Circuit collapsing and potential destruction due to excessive supply current

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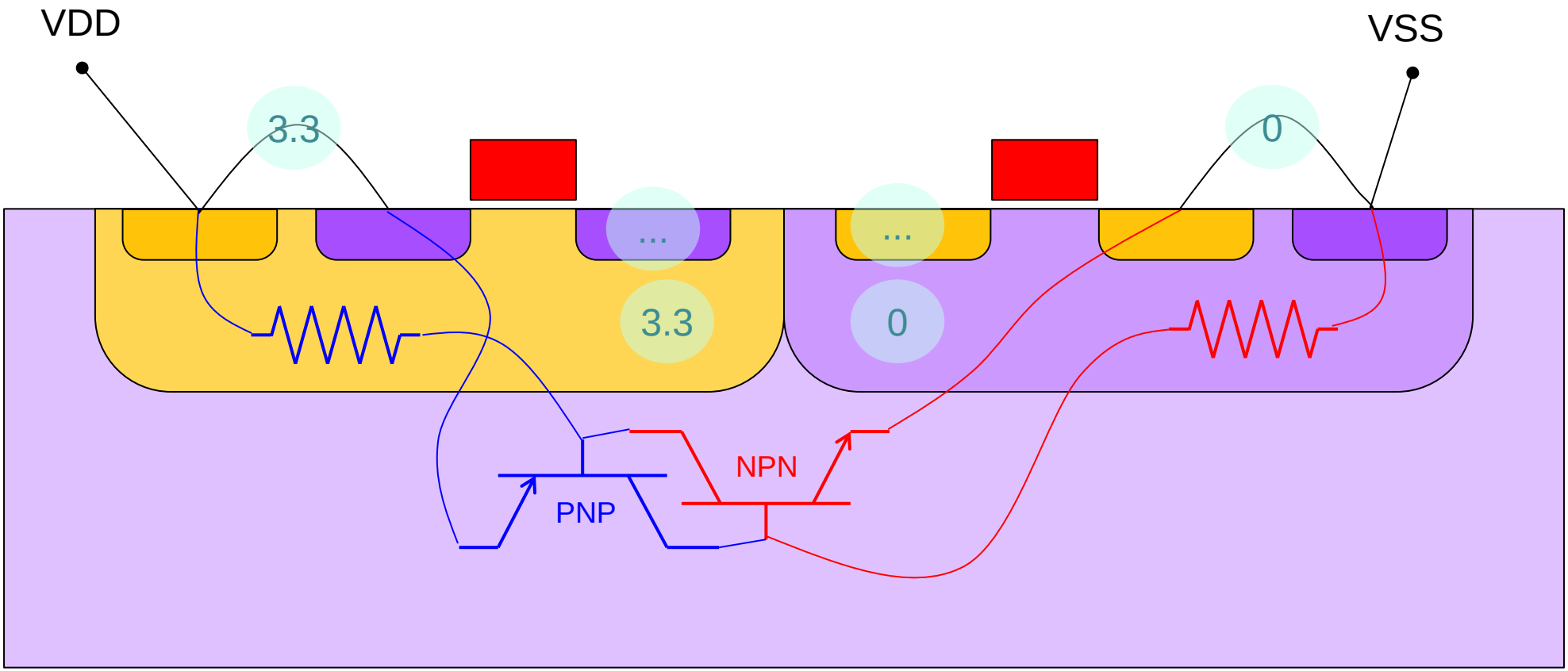
Bulk CMOS has an annoying thyristor



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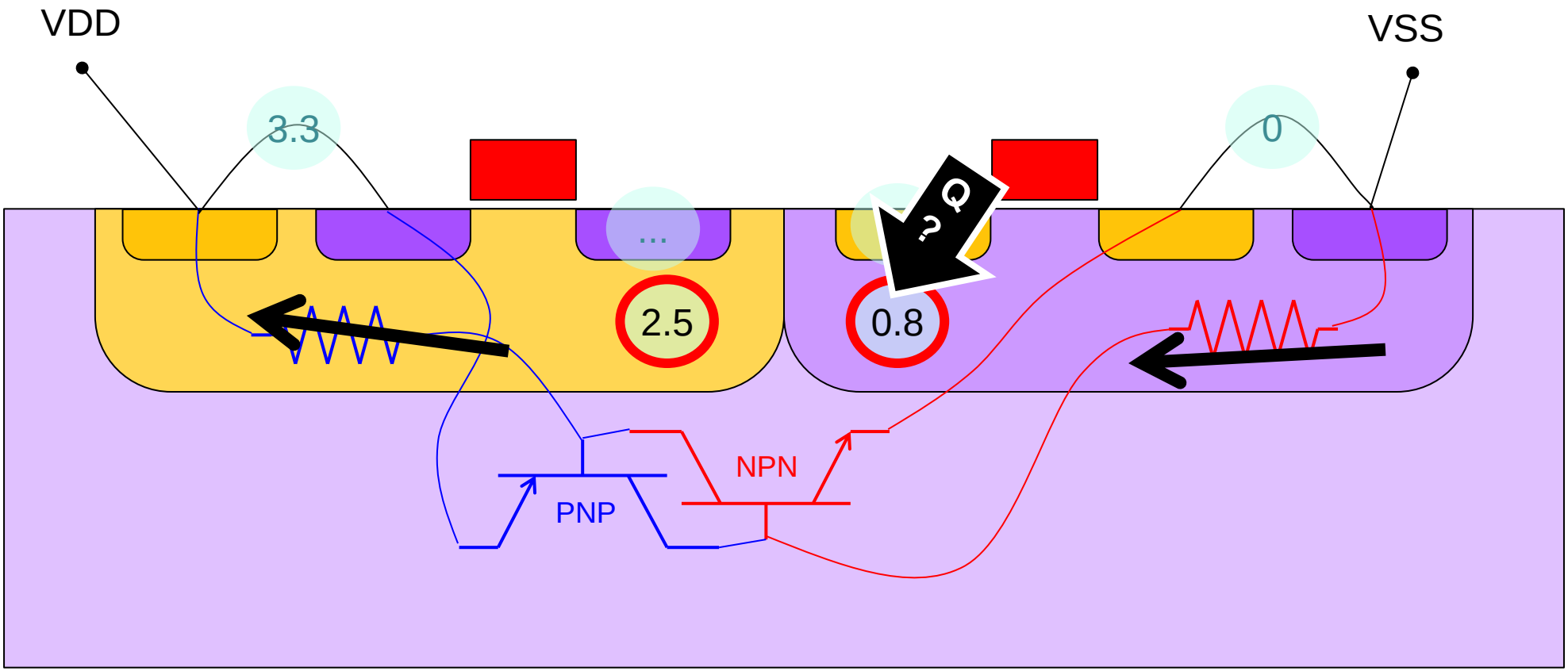
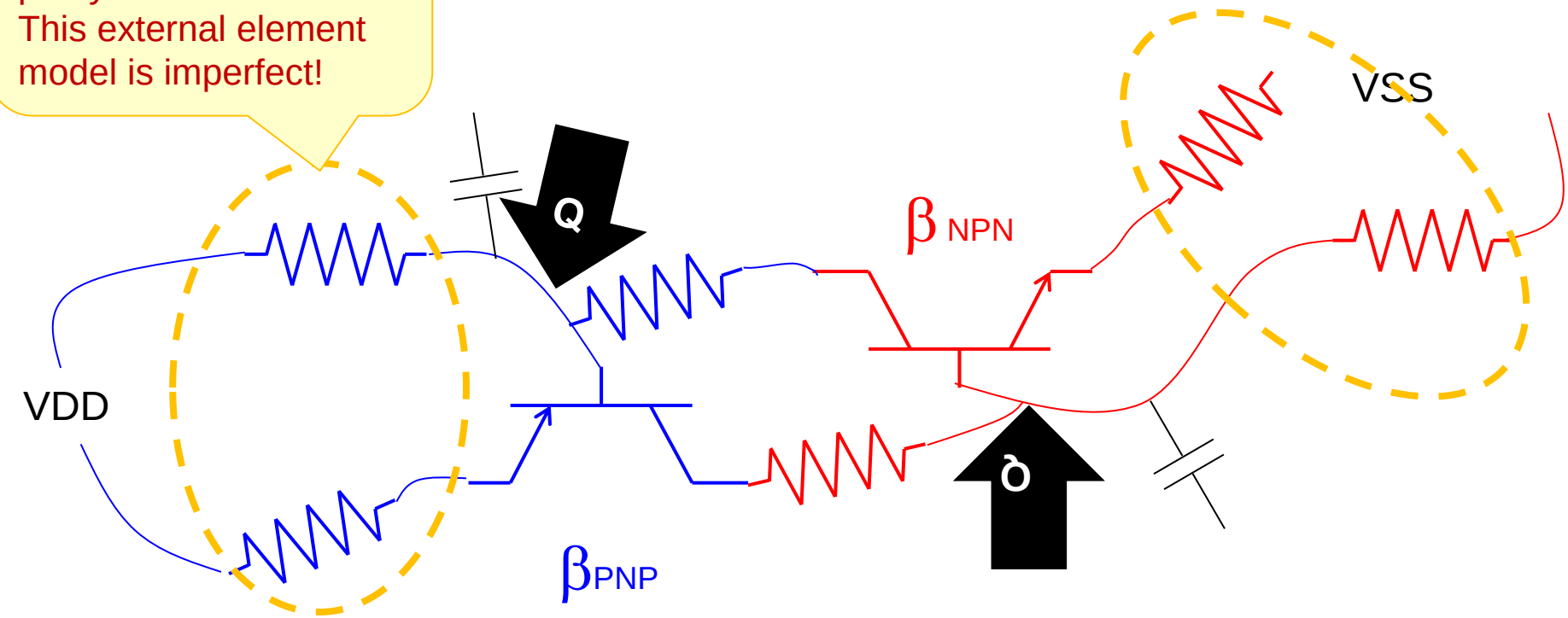
Bulk CMOS has an annoying thyristor



Thyristor = 2 * BJT

Attention: these two resistors are physically partly the same
This external element model is imperfect!



- Threshold for ignition: Q, C
- Conditions for sustaining: β, R

Modeling SEL

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- Quantitative compact (=SPICE) model?
  - ⇒ Much better: a 3D device simulator.
- What lacks: value for series resistances
  - ⇒ Series resistances in E, B, C. Can estimate it from techology data.
  - ⇒ Pay attention that “resistance” applies to majority carriers. Base resistance is thus over/underestimated and partly uncorrelated
  - ⇒ Emitter and Base resistances partly overlap: Emitter current increases IR drop of Base.
- What lacks: models of the parasitic BJTs
  - ⇒ β: must eventually “measure” that. Start with default value (100...1000) for “qualitative” estimate.

Design countermeasures

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Avoid ignition

- ⇒ minimize sensitive volume
- ⇒ maximize C/Q: increase node capacitances

Avoid sustaining

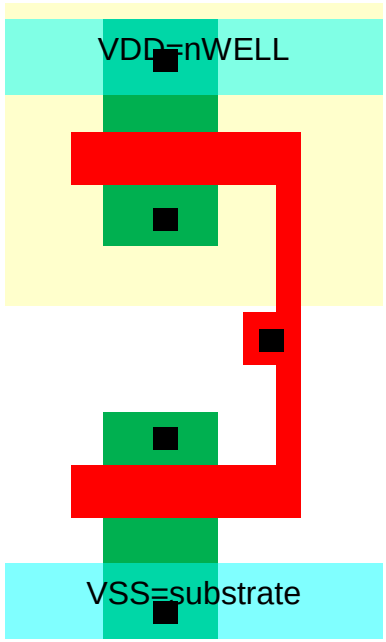
- ⇒ Maximally reduce the series resistance in the thyristor
- ⇒ Between the nWELL and pWELL: guard rings metallically tied to VDD/VSS

Avoid proliferation

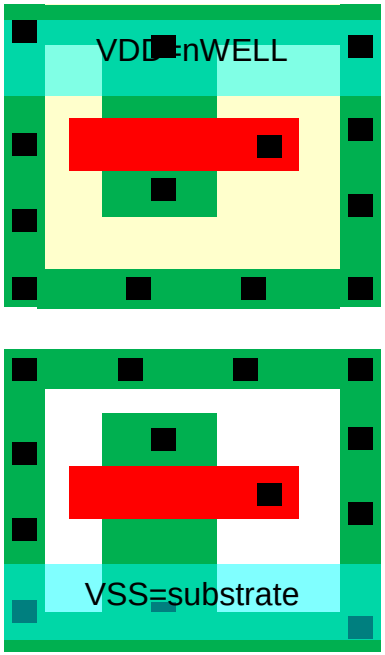
- ⇒ nWELLs (actually the well not being the substrate) should be fragmented. So that the latchup remains confined: when one section latches, the general supply voltage does not collapse.

Design style

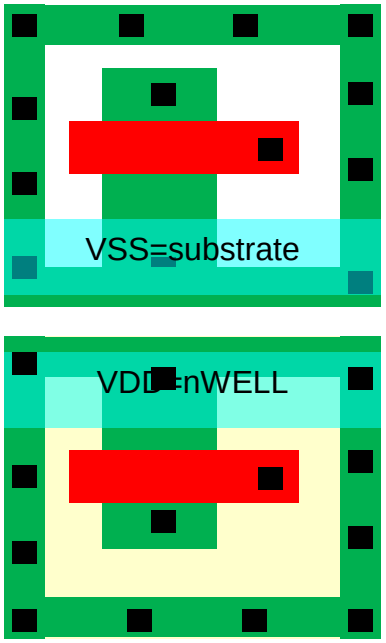
Classic CMOS design style



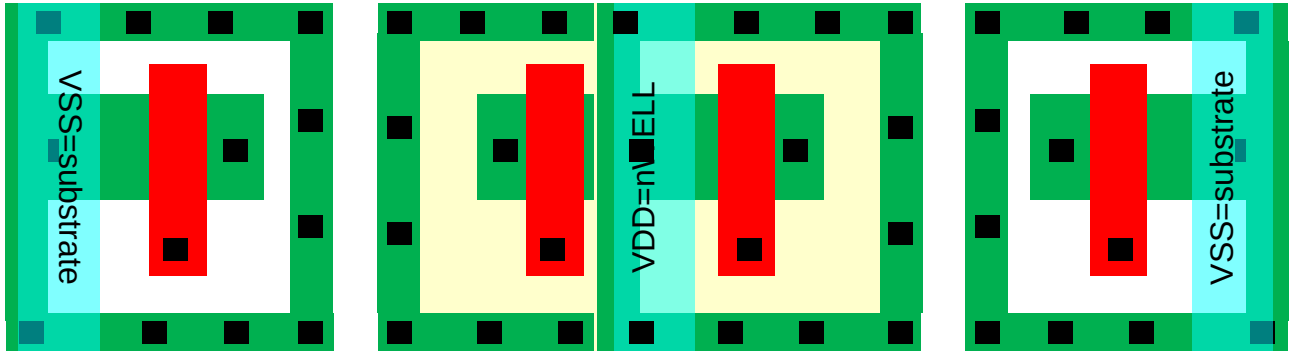
Metal guardring around wells

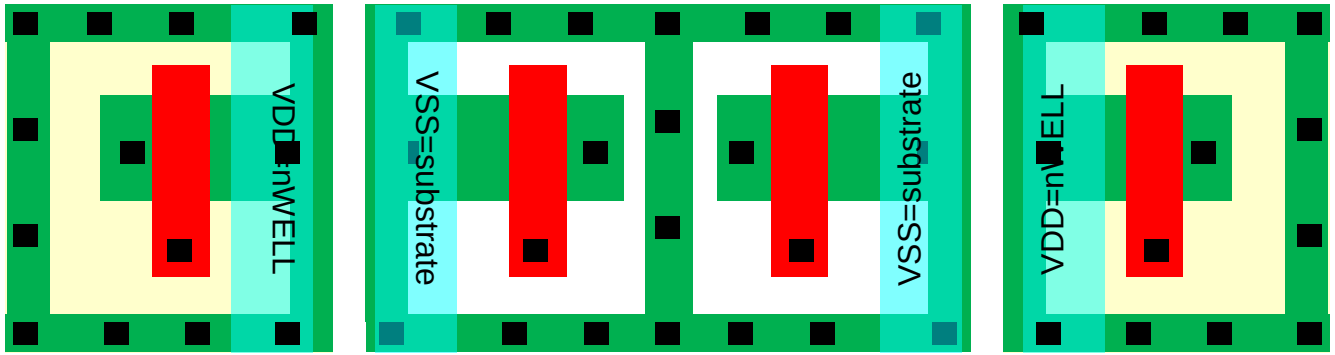


Rails in the middle



Mirrored rails





Technology measures

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- Avoid the thyristor
  - ⇒ SOI, FinFET
- Reduce the bipolar feedback
  - *Poor* BJTs
  - ⇒ Trenches
  - ⇒ Low sheet resistances
  - ⇒ Epi wafers (p- on p++ or n- on n++): reduces 1 Base resistor
  - ⇒ Increased recombination → reduces minority current and increases I_{dark}
- Reduce the pick-up
  - ⇒ Small charge collecting volume in the Bases

Triple well...

The number of *possible* thryristors increases

Good to know

- nMOS-only or pMOS-only circuit parts cannot latchup.
- A standalone BJT does not latchup

SEL and vulnerable nodes

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⇒ How much charge is deposited on a vulnerable node

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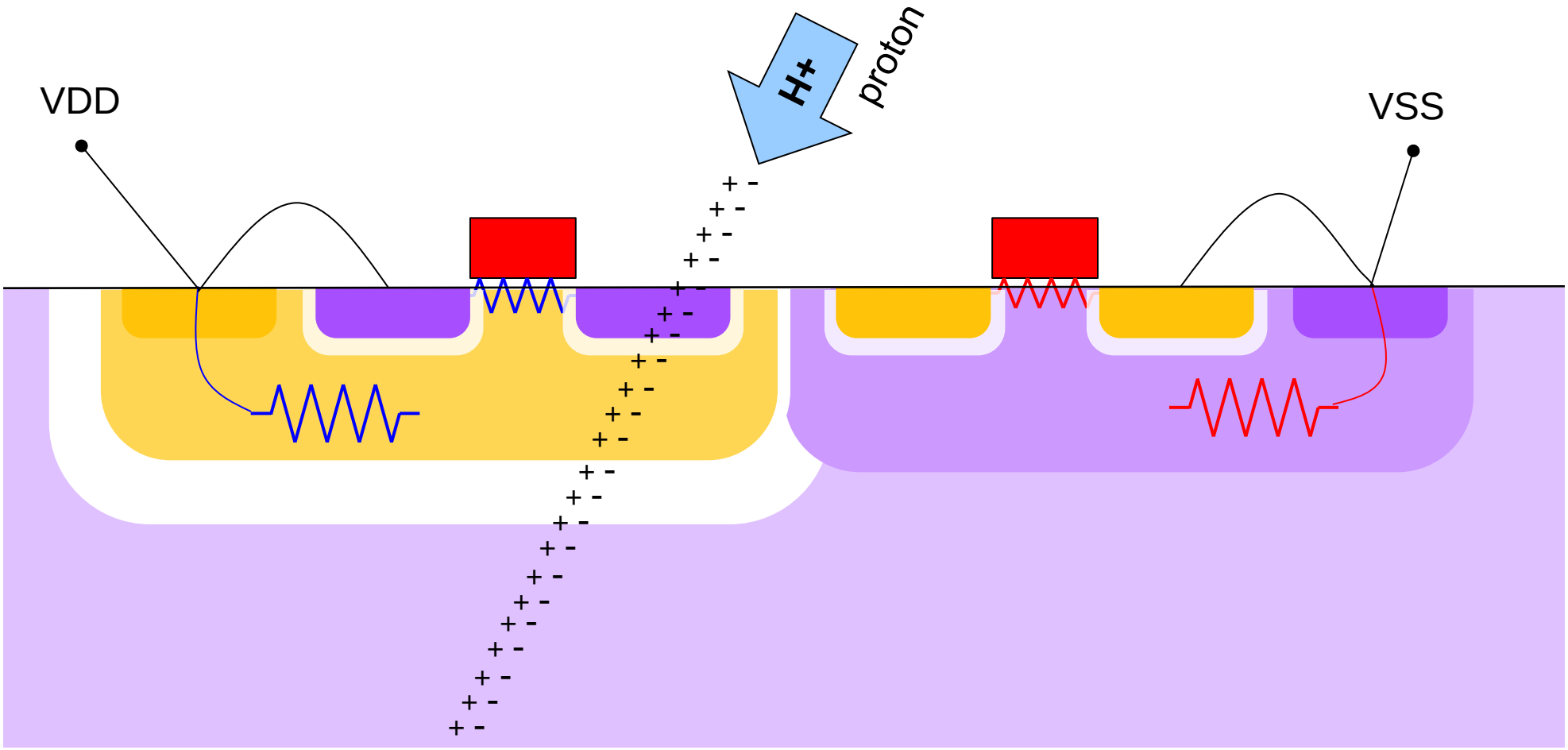
Vulnerable volume @t_0



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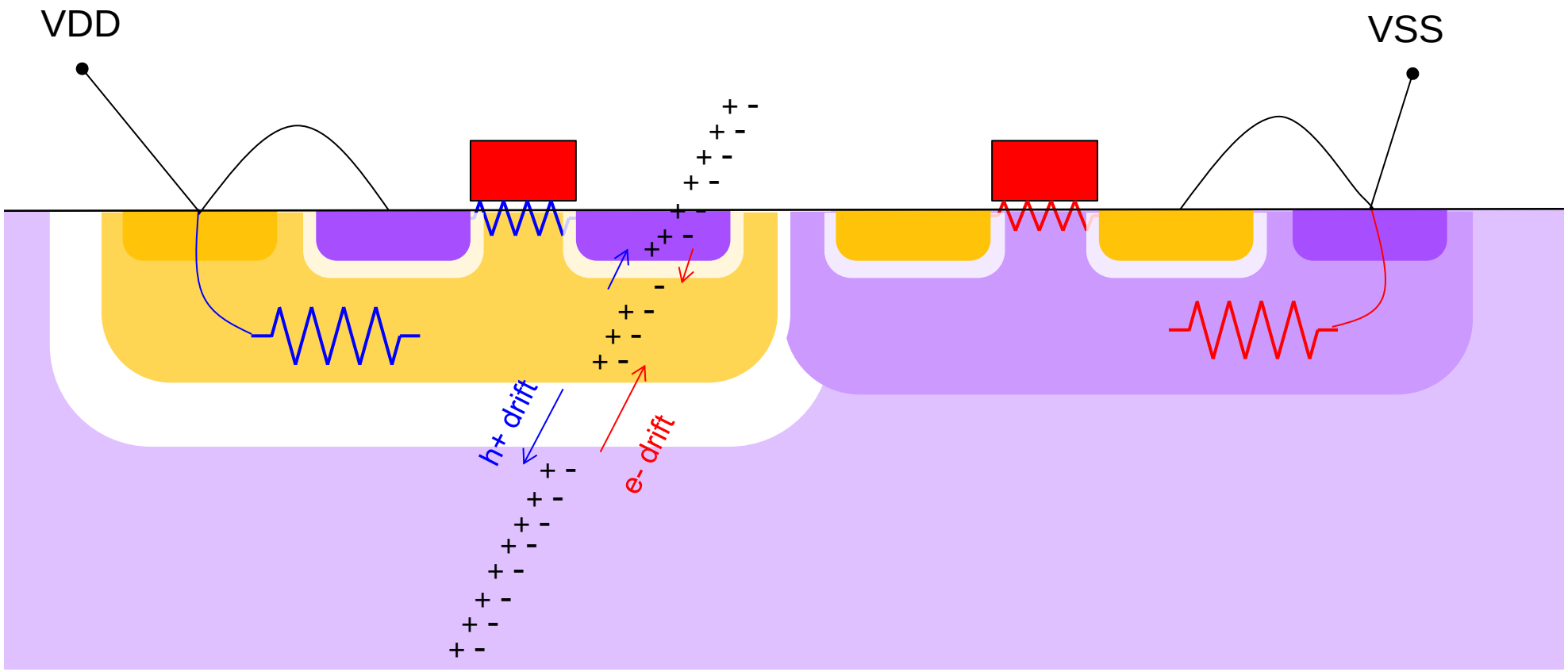
Vulnerable volume @t_0+10ps



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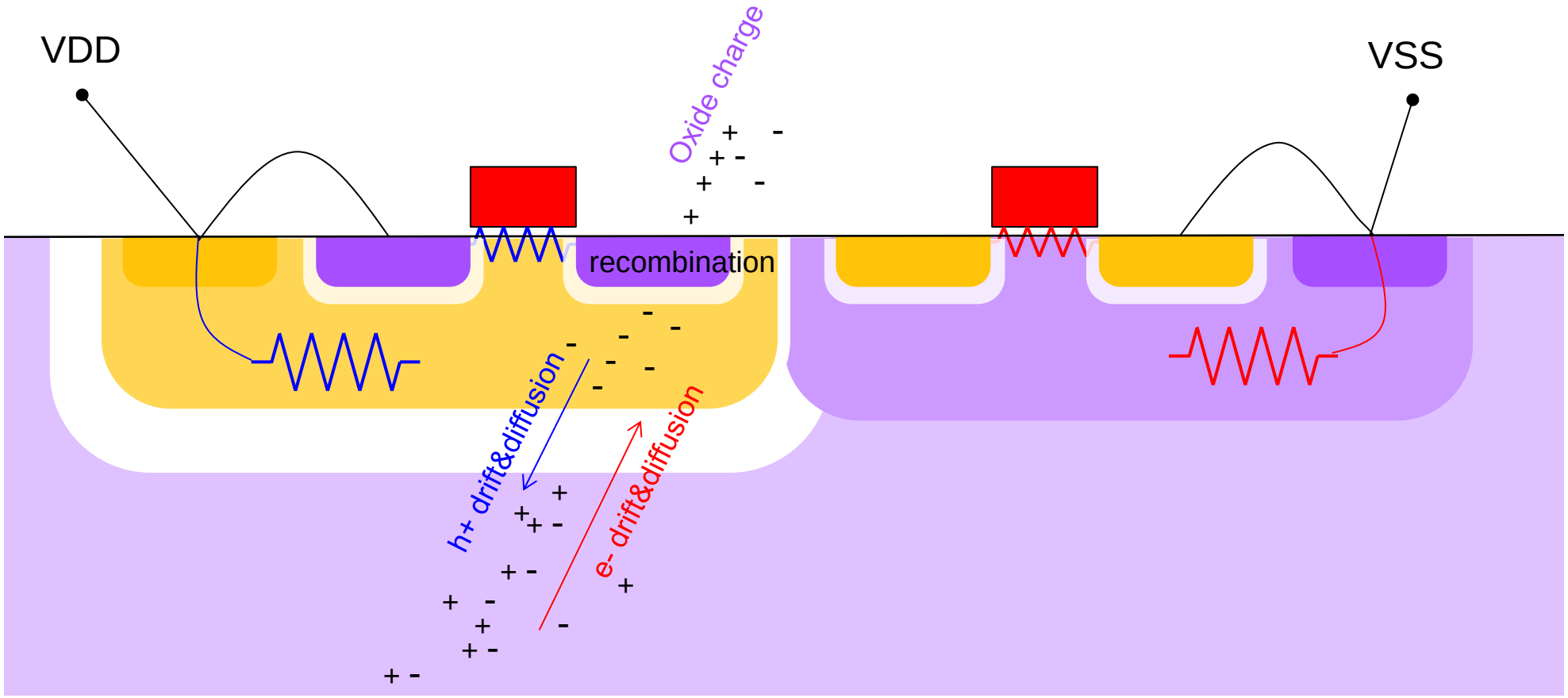
Vulnerable volume @t_0+0.5ns



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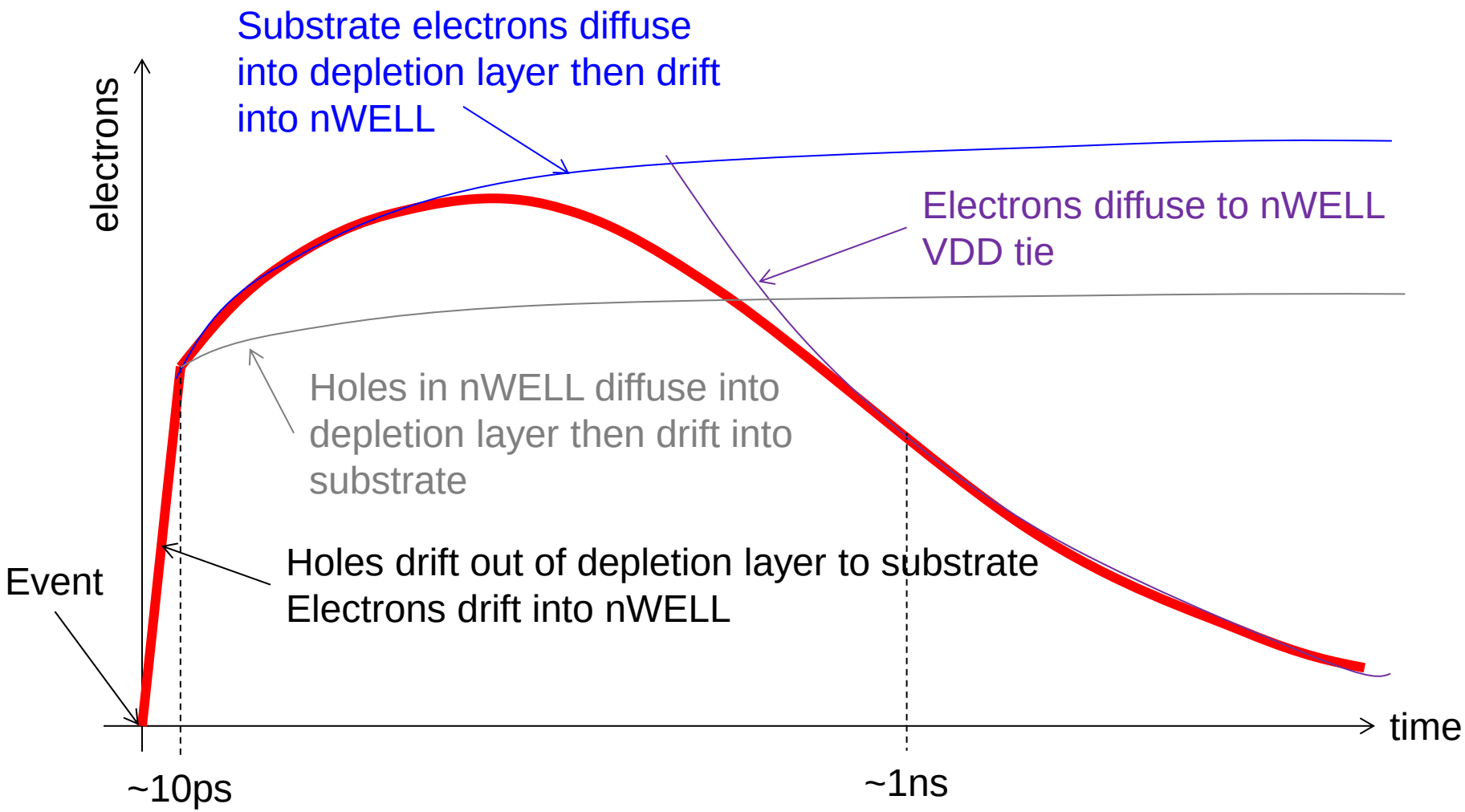
Net node charge as function of time

the nWELL case



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LET linear energy transfer

Heavy ions are commonly described by amount of energy lost per unit track length = Linear Energy Transfer

Linear Energy Transfer

- ⇒ Energy loss per unit path length
- ⇒ dE/dx= MeV/cm
- ⇒ Divide by material density = MeV.cm^2/mg
- ⇒ LET of 100 MeV.cm^2/mg corresponds to charge deposition of 1pC/µm = 6E6 e-/h+

How does LET spectrum relate to the real space environment?

- ⇒ A measure for the heaviest ions/events that can be expected
- ⇒ Says nothing about number of particles or probability

e-h+ pairs per µm

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100 MeV.cm^2/mg ≈ 1pC/µm = 6Me-h+/µm

⇒This is a linear function, thus 50 MeV.cm^2/mg is still 3 million charges/µm.

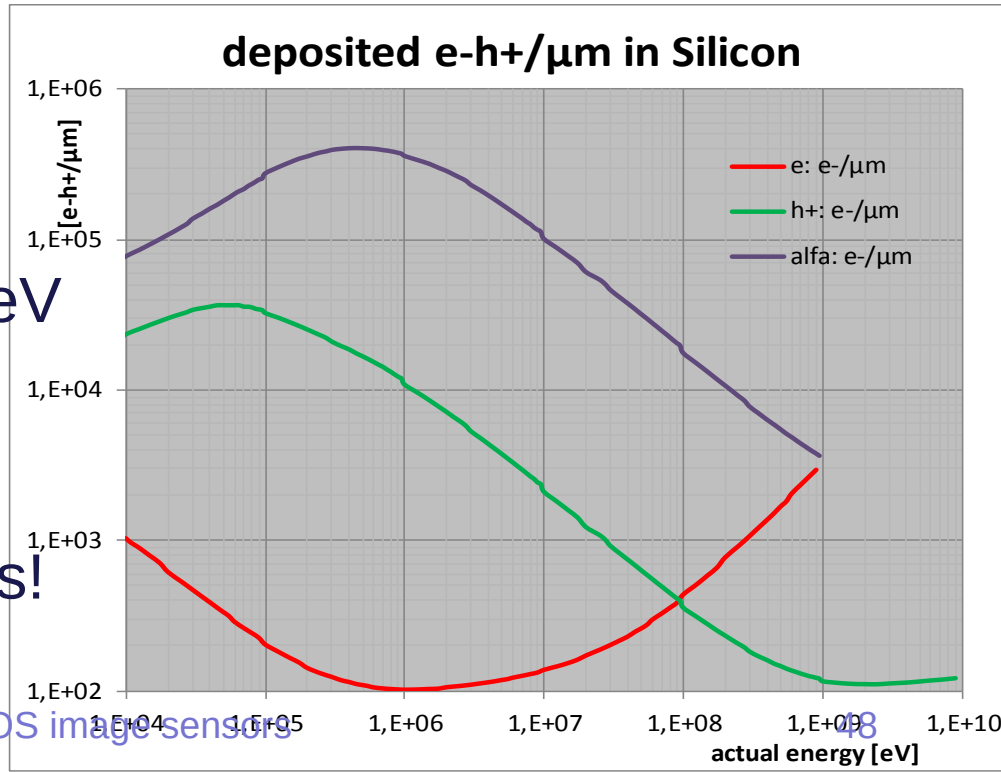
For reference /µm

⇒α: 4E6 eh, max @1MeV

⇒H+: 30000 eh, max @80keV

⇒β (and γ): <5000 e-h+

⇒*More* energy: *less* charges!



Voltage drop

assuming instantanous charge deposition

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- Minimal junction size and capacitance
  - ⇒1fF & 1µm: 6000 e- = 1V
  - ⇒Electrons (hence gamma) cannot create $V_{forward}$
  - ⇒Protons can (marginally) ignite LU
- Proton SEL hard junction?
  - ⇒5fF & 1µm: 30000 e- = 1V. Yet, shallow angle?

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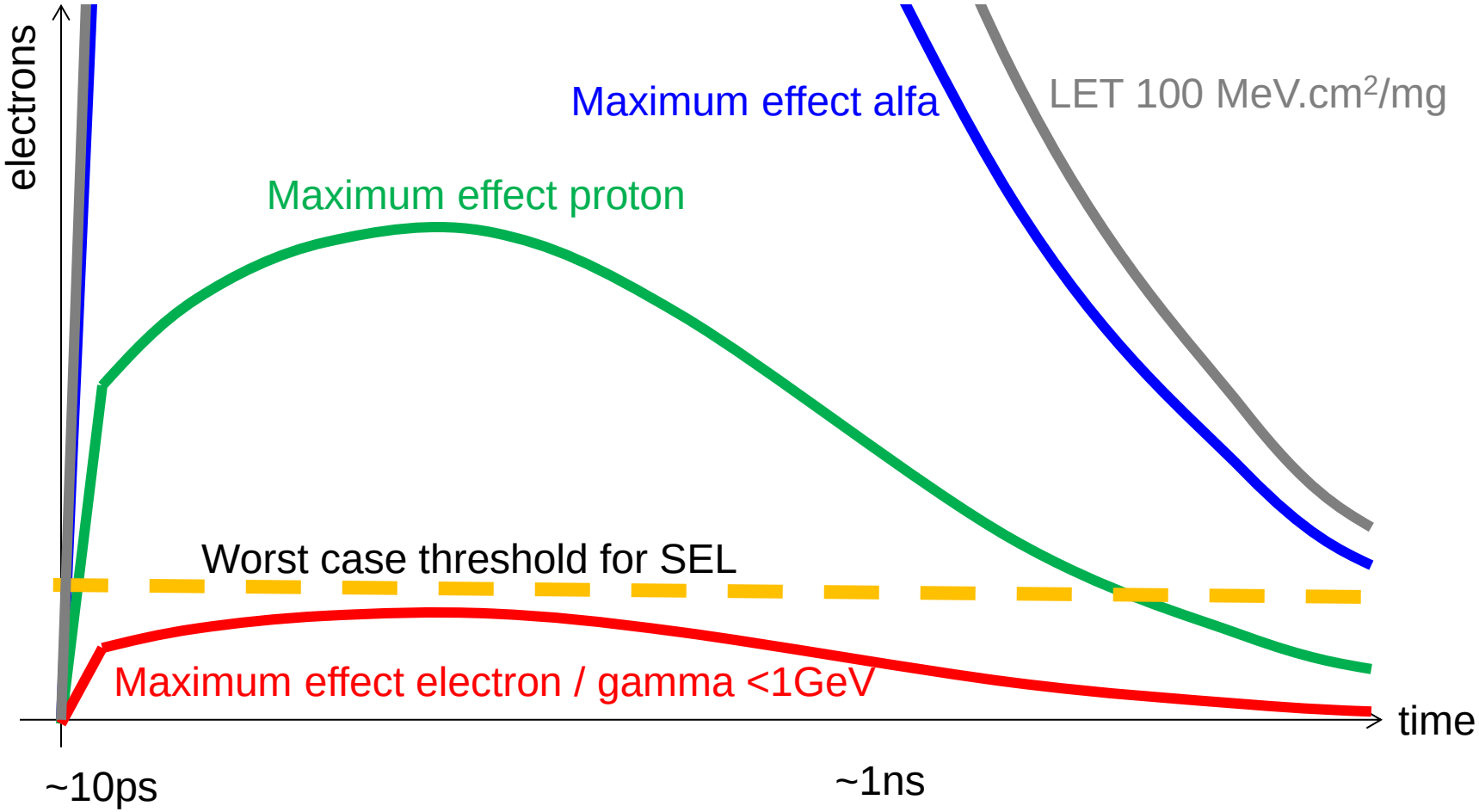
Net node charge as function of time



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Take home message

conclusions

Take home

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CMOS imagers can be made hard against TID, SEL, SEU etc by design

⇒TID: avoid field leakage

⇒SEL: reduce bipolar feedback

⇒SEU: vulnerable volume & circuit redundancy

Photodiode hardening for SE and displacement damage remains a question

- Photodiode redundancy?

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Thank you