caeleste

CMOS Detector Workshop
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Development of signal acquisition Prototype ASIC for Large Format NIR/SWIR Detector Array

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Selex ES

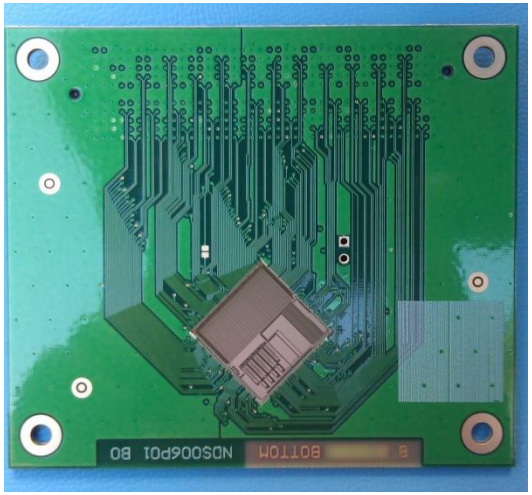
esa

easics

status

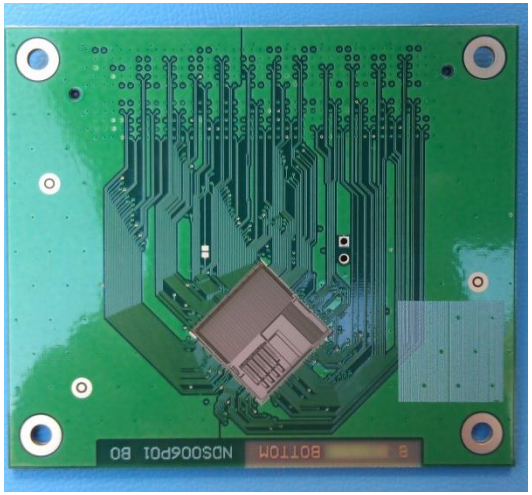
- **Development in two phases:**
  - Prototype ASIC (2013)
  - Room temperature testing in progress
  - Cryogenic temperature testing Q1 2014

  - Final product design (2014-2015)



Outline

- **Motivation and technical challenges**
- **Design for Radiation hardness and Cryogenic temperature**
- **Circuits**
- **Test setup**
- **Test results**
- **Conclusions**



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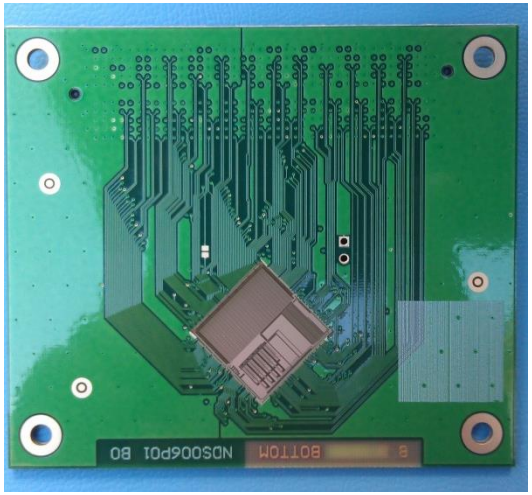
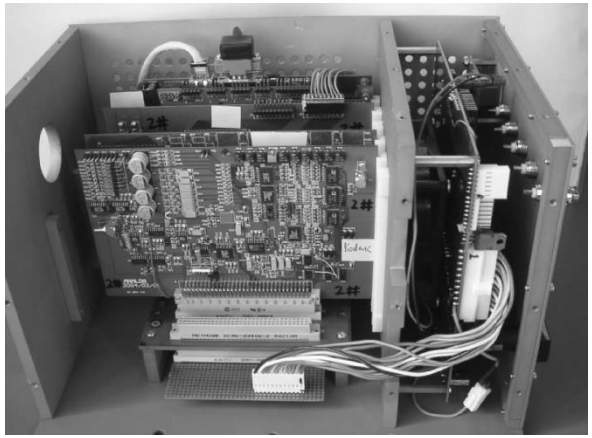
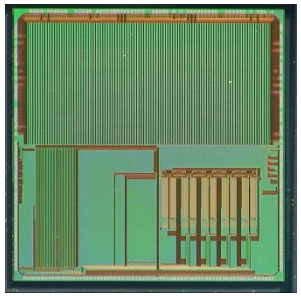


Why an ASIC ?

Data acquisition and control system for IR imagers





Analog domain

- Signal conditioning
- Analog to digital converter
- Regulated power supply
- Bias voltage/current references

Digital domain

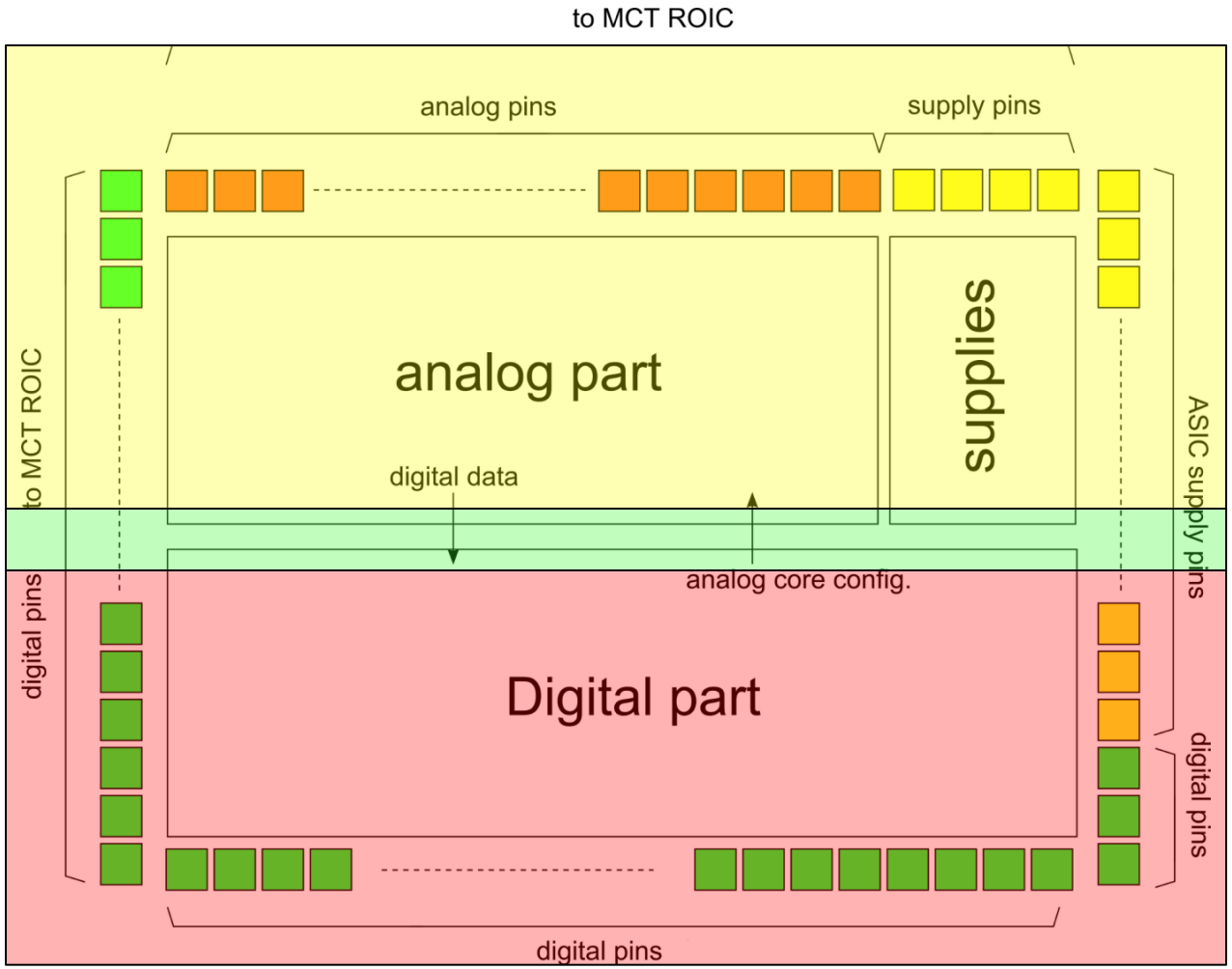
- Digital control core
- Memory & Clock
- Data Communication

A signal conditionning ASIC

This development aims at providing the community with a signal conditioning ASIC

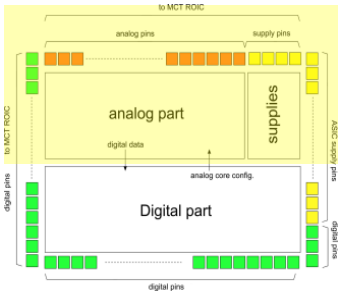
- **Tailored to imagers (especially IR sensor)**
- **Versatile**
- **Wide operating temperature range**
- **Multiple IR detectors**
- **Multi-sensor systems**

A mixed mode ASIC



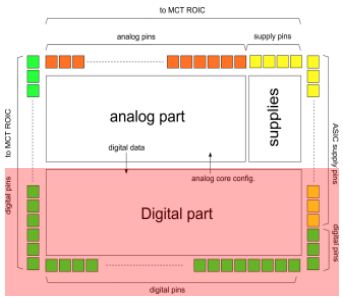
Challenging specifications

Analog domain		
Function	**No.**	**specifications**
LDO	4	1.3-3.4 [V], 100mA max. supply current **Tested @ room temperature**
Analog inputs	16	
Preamplifier / CDS / Offset cancellation	4	5 gains, 25uV RMS noise 8 bits Offset removal
16-bit ADC	4	Successive approximation with bits calibration Target DNL < 1,5 LSB
ROIC bias and Reference voltages	16	10 bits, rail to rail operation **Tested @ room temperature**
ROIC health monitoring	4	Resistors / differential voltage monitoring 16 bits
Internal reference	1	1.2V Bandgap **Tested @ room temperature**
Temperature sensor	1	**Tested @ 10-40°C**



Challenging specifications

Digital domain	
Master clock	0 – 200 MHz
System level protocol	2 – 200 Mbit/s Space Wire **Tested directional @ room temperature**
ROIC digital control	32 **Tested @ room temperature**
Scheduler time granularity	10M updates/s
Sequence nesting depth	8
ROIC monitoring and trigger inputs	8 **Tested @ room temperature**
ROIC programming channel	1 SPI **Tested @ room temperature**



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Radiation hardness approach

Radiation hardness: digital design

DARE Library for digital design

- Developed by IMEC
- Designed up to Mrad, used in flight models
- DARE180 (UMC 0.18um 1P6M CMOS)
- Radiation Hard Standard Cells, SRAM, I/O cells, PLL

Radiation hardness: digital design

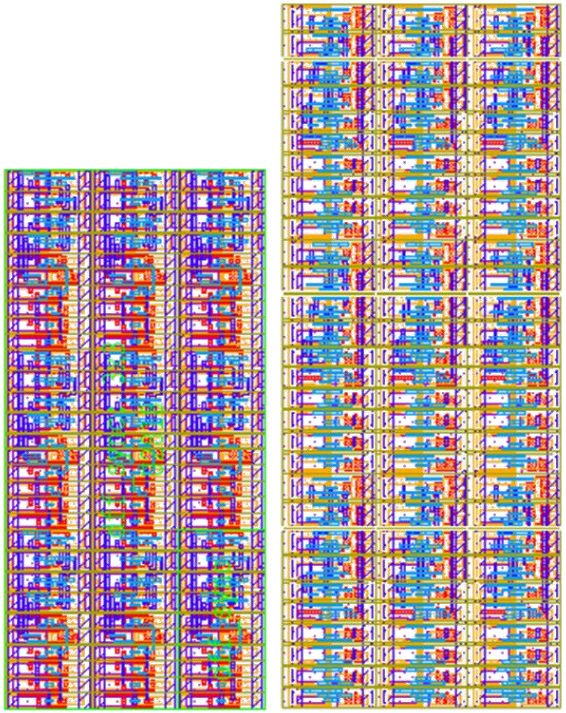
Circuit topology is rad hard:

- Redundancy
  - Hamming Codes
  - Parity check
- Watchdog Timers

Radiation hardness: analog design

Caeleste radhard library

- Analog and High Voltage logic standard cells
- Combined with custom tactical cells



Layout using Caeleste's standard library (left) and the same in the fully radiation hard library (right)

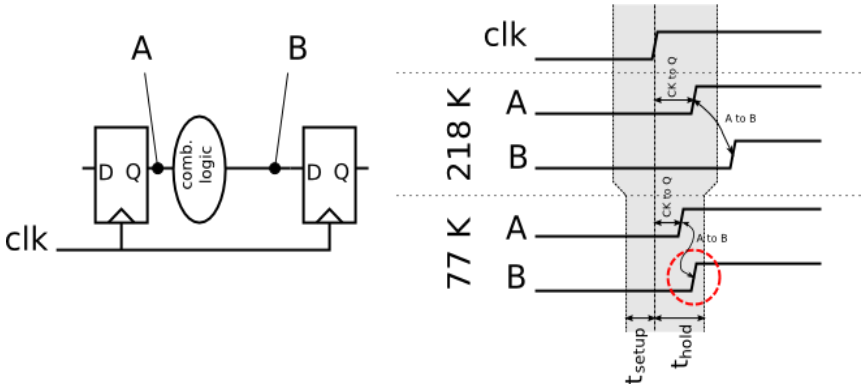
Design for low temperature

Analog and digital flow require different approach on modeling and design strategy for cryogenic temperature

Cryogenic digital design

The DARE library has never been used at 77K

The logic becomes faster. However one must take care of set-up and hold time violation.

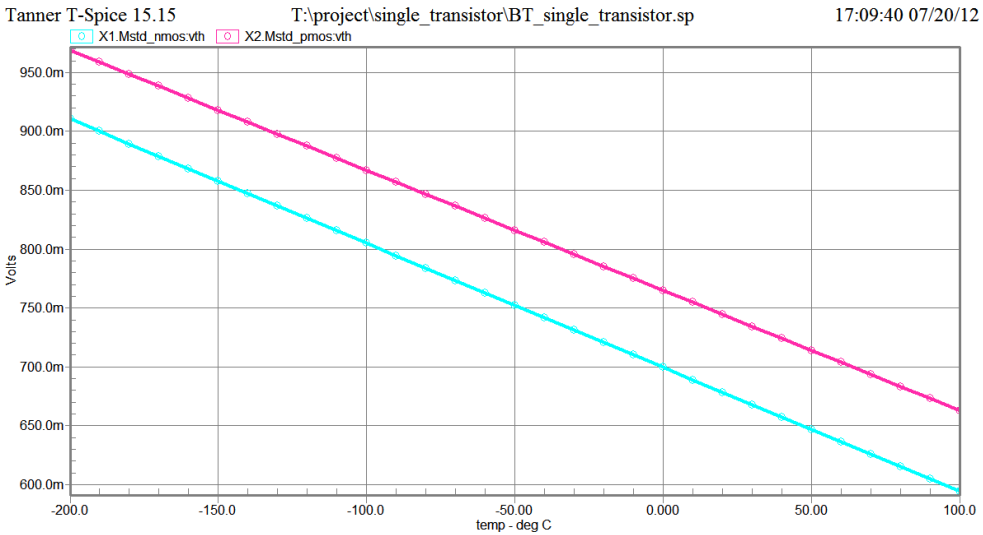


The library models have be adapted, based on a model characterized at 218K

Other components like SRAM are also to be validated

Cryogenic analog design

- MOSFET modeling
  - V_{th}: increase
  - Mobility: increase
  - MOS switch: low R_{on}



- Careful choice of passive components

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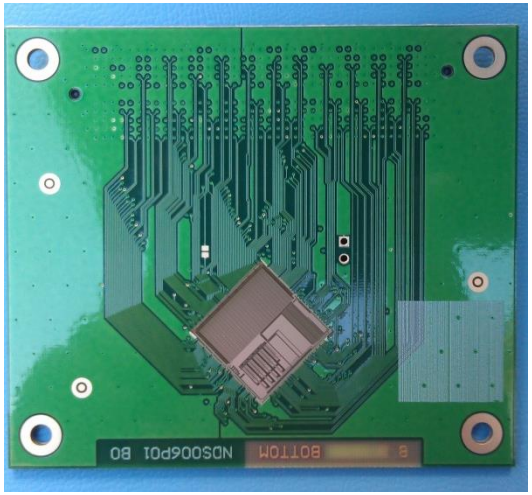
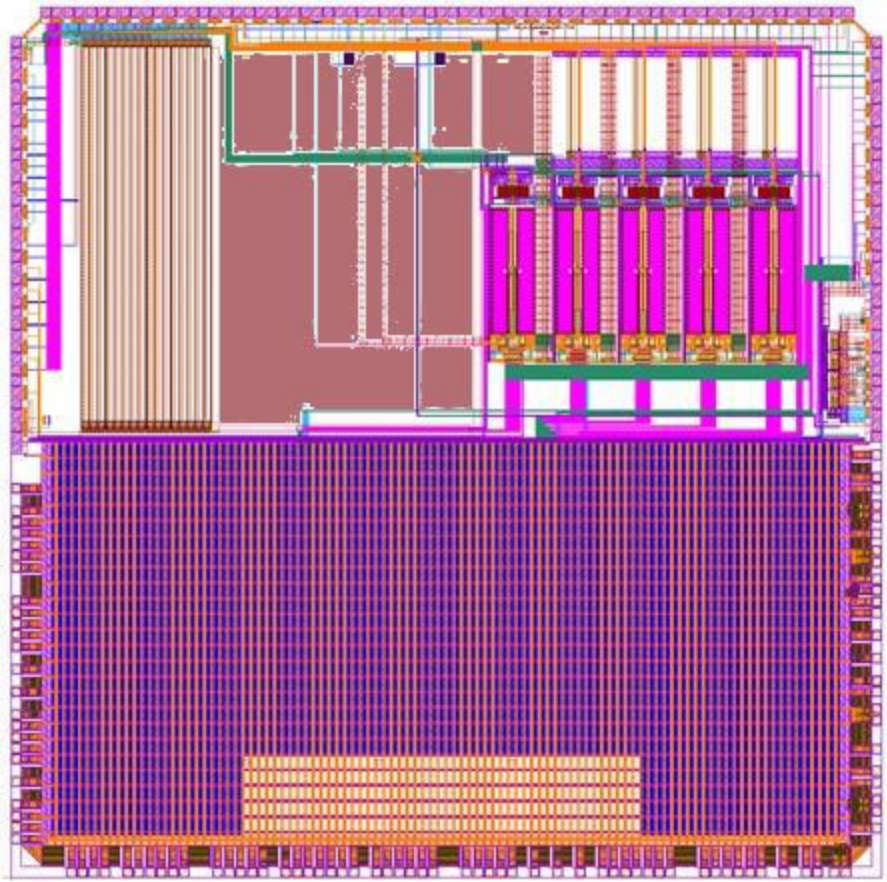
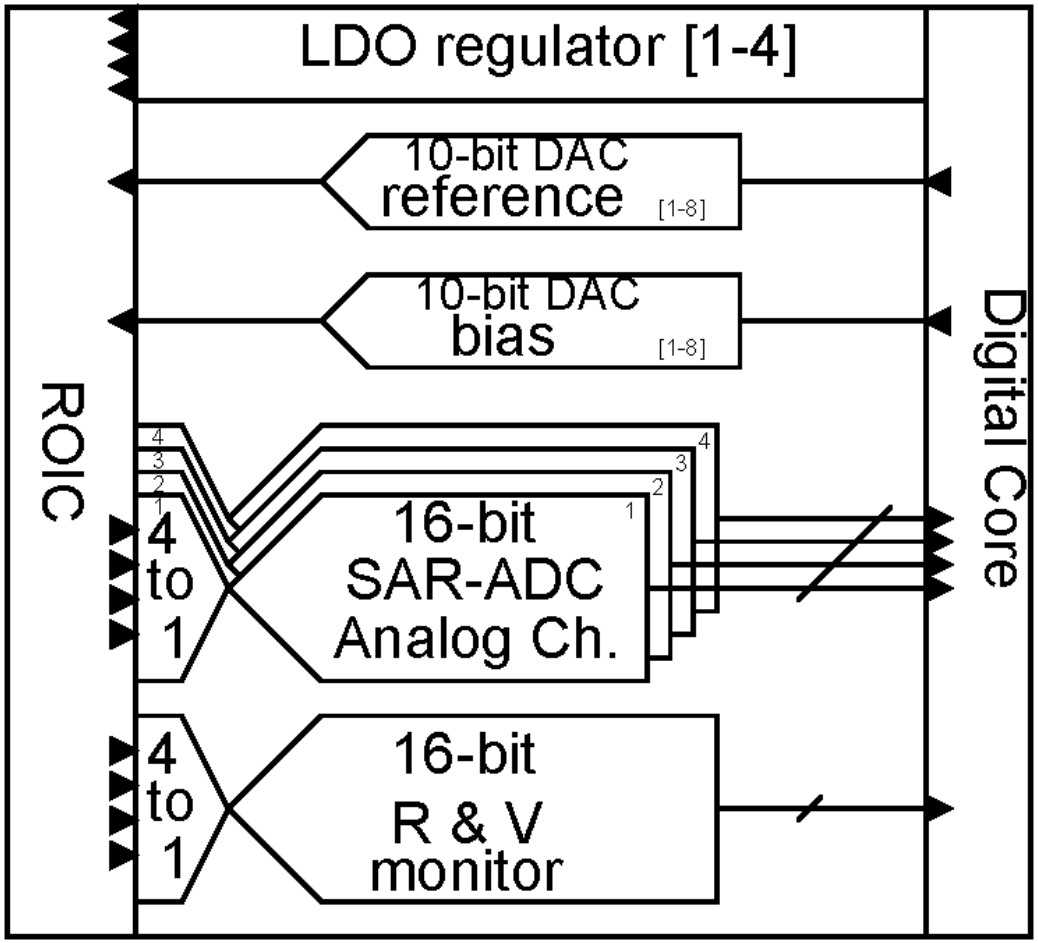


floorplan

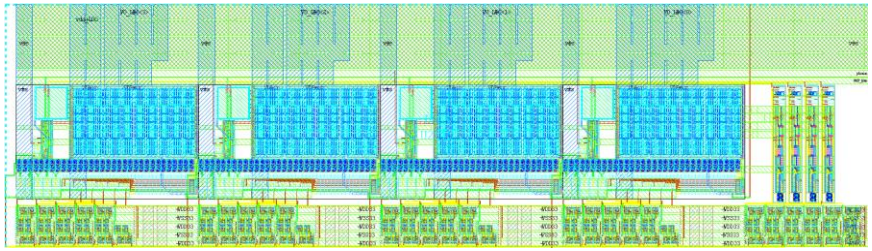


Analog section

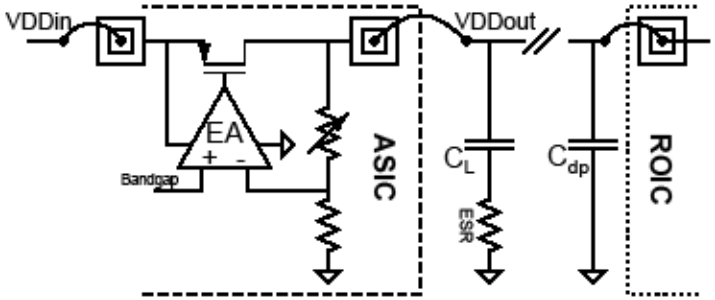


LDO

- LDO
  - Programmable output
  - Output current 0-100mA

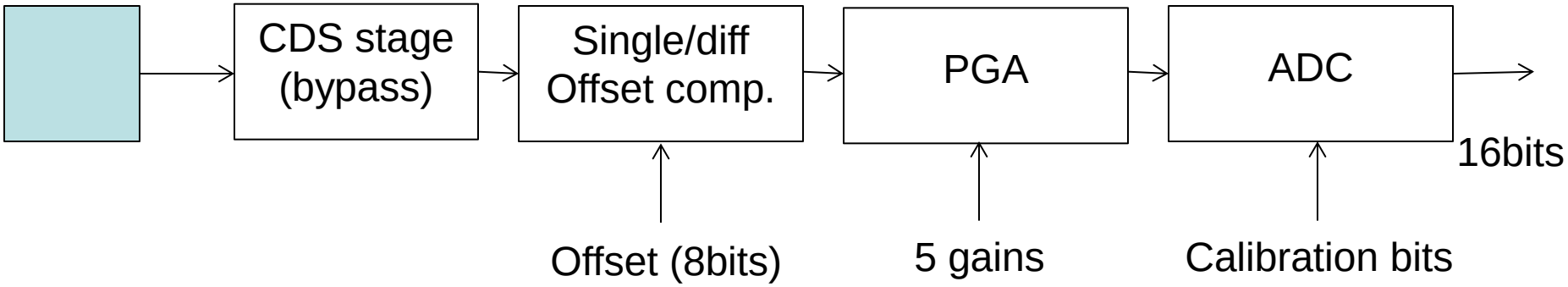


- Bandgap
  - 1.2V
  - 77K-300K

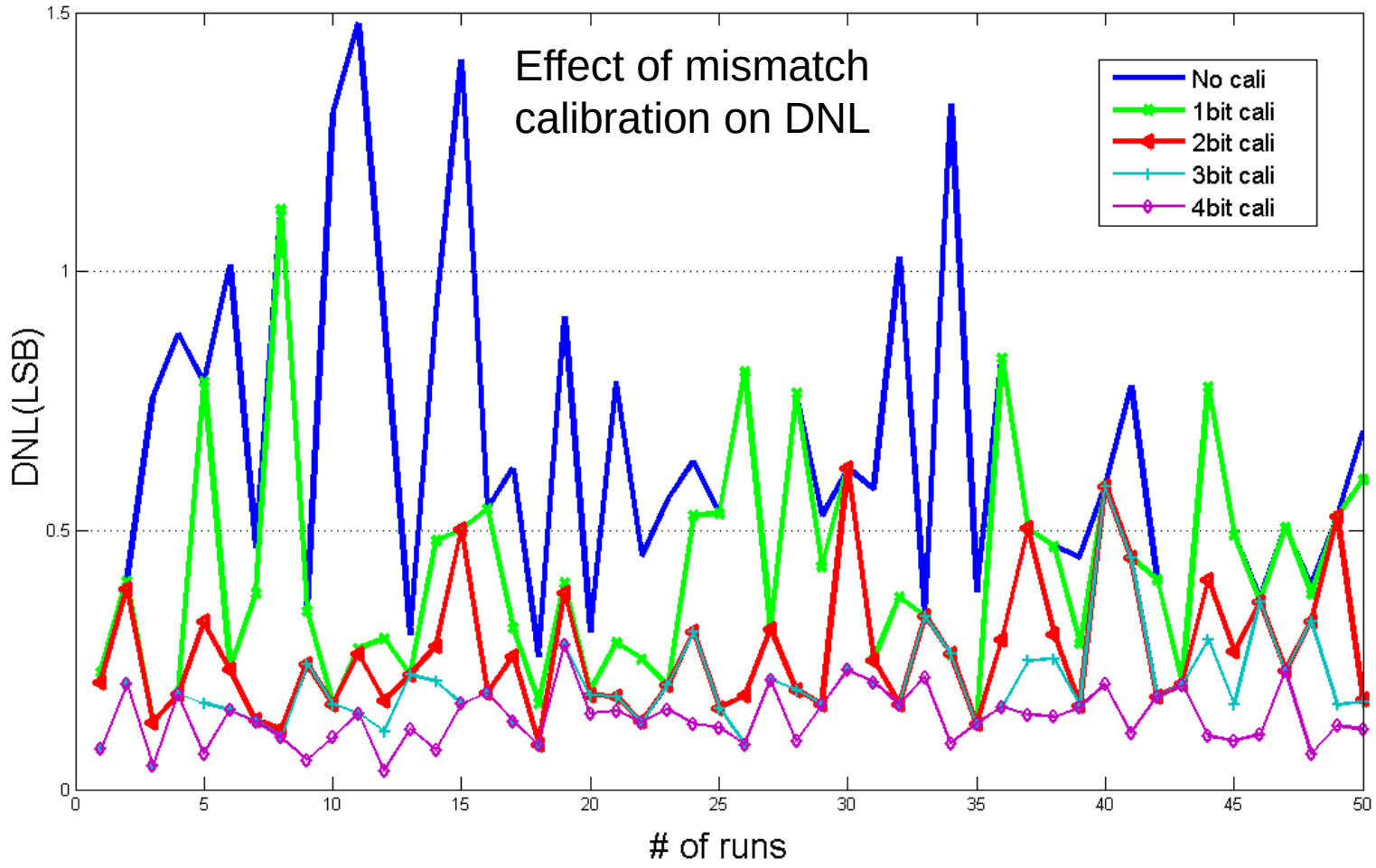


Conversion chain

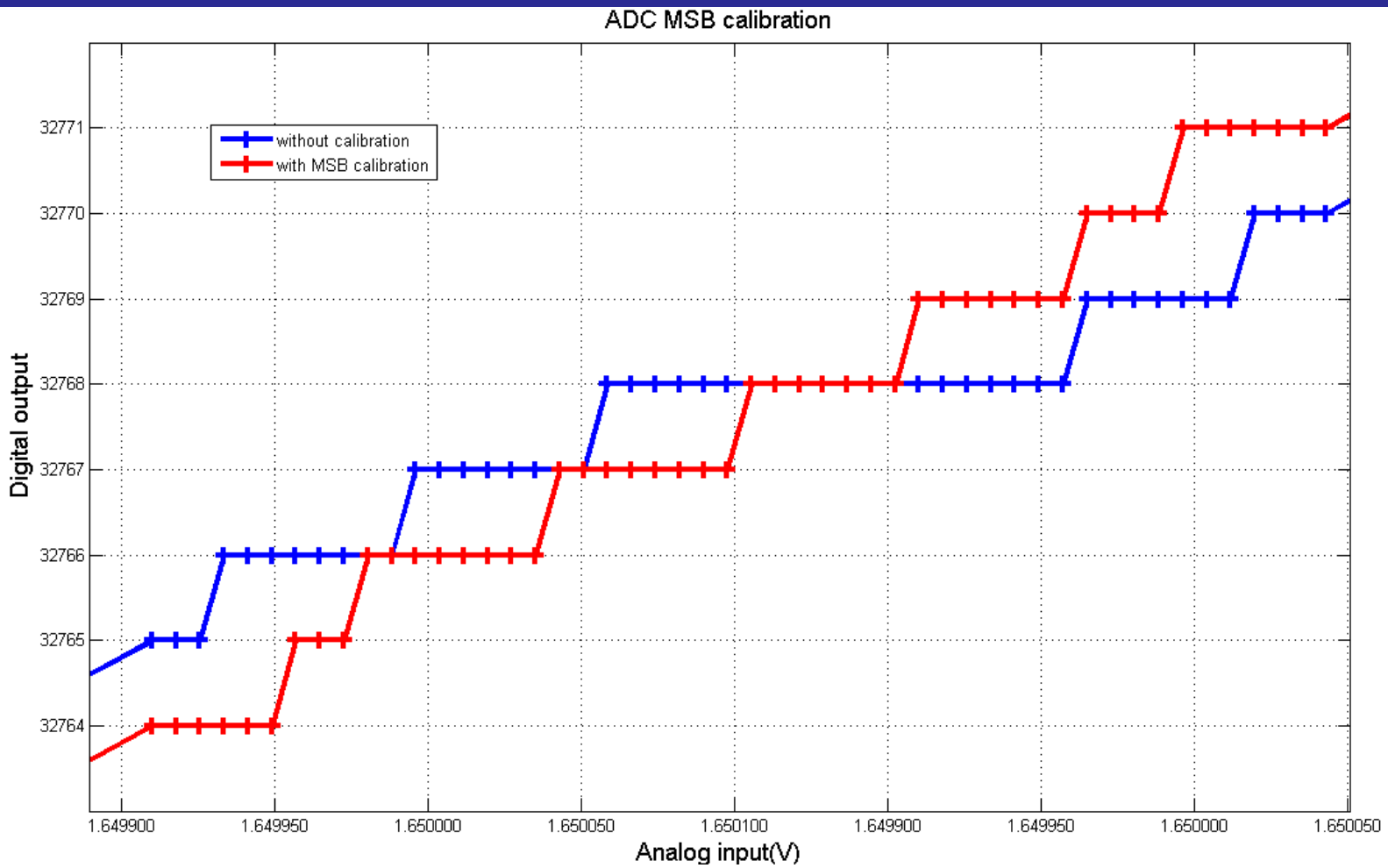
- 16-bit, 50-200kHz, fully differential SAR ADC
  - Hybrid configuration Resistive / capacitive
  - Low offset comparator: auto zero
- A calibration scheme to cover the wide temperature range



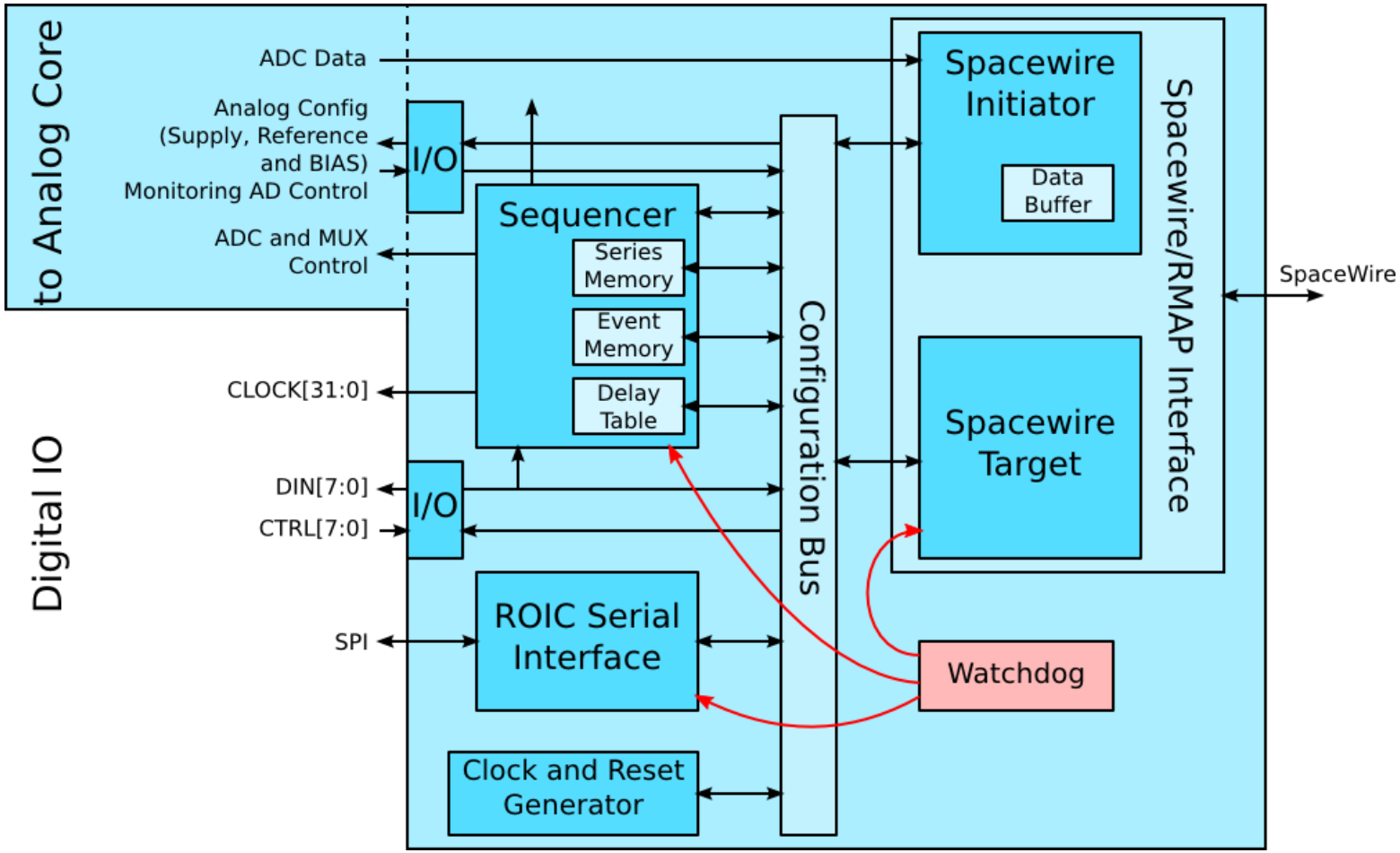
ADC: model driven design



ADC: design verification

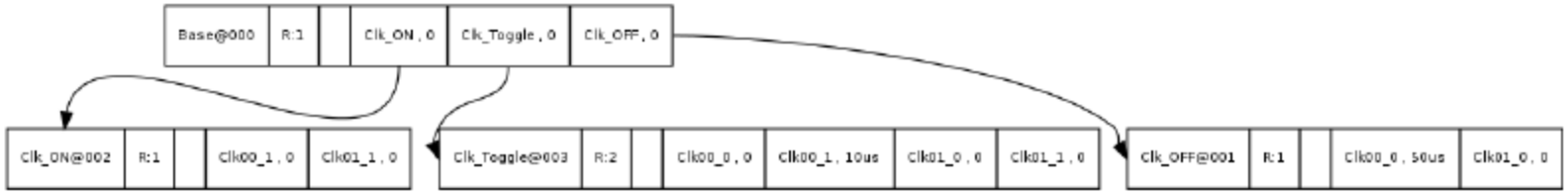


Digital design



Digital design

```
### Series Table
##########                    Repeat  Addr
#################################################################################
S Base                                1    0
T       0          Clk_ON
T       0          Clk_Toggle
T       0          Clk_OFF
S Clk_ON 1
T       0          Clk00_1
T       0          Clk01_1
S Clk_Toggle2
T       0          Clk00_0
T    10us          Clk00_1
T       0          Clk01_0
T       0          Clk01_1
S Clk_OFF1
T    50us          Clk00_0
T       0          Clk01_0
```



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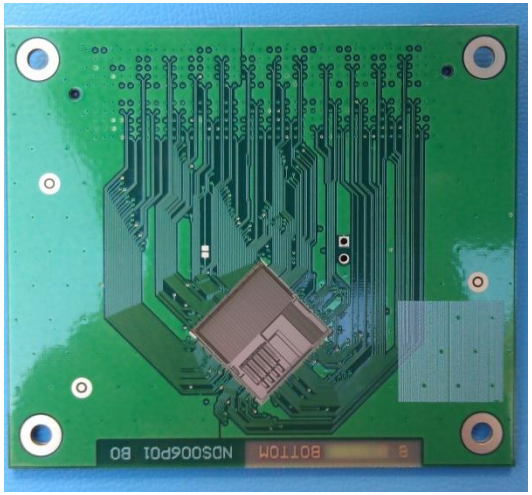
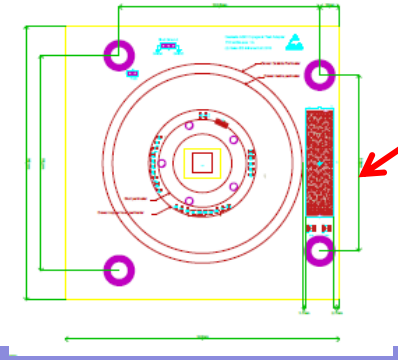
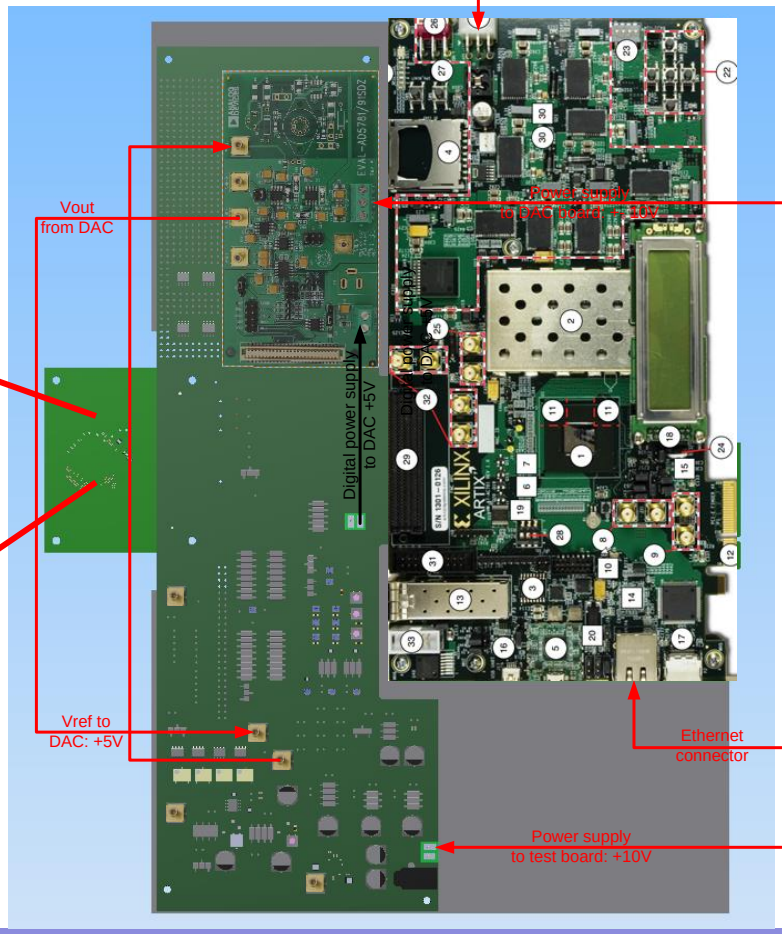


Test setup

<u>Unified design for:</u>
Room temperature
Cryogenic temperature





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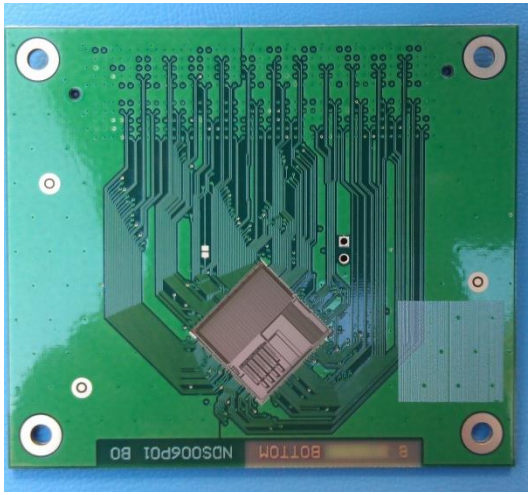


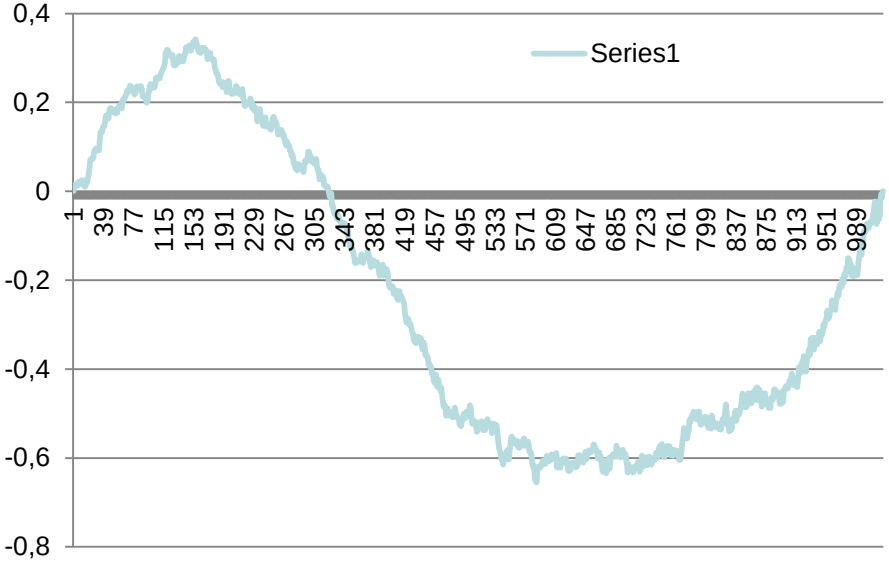
Tests results

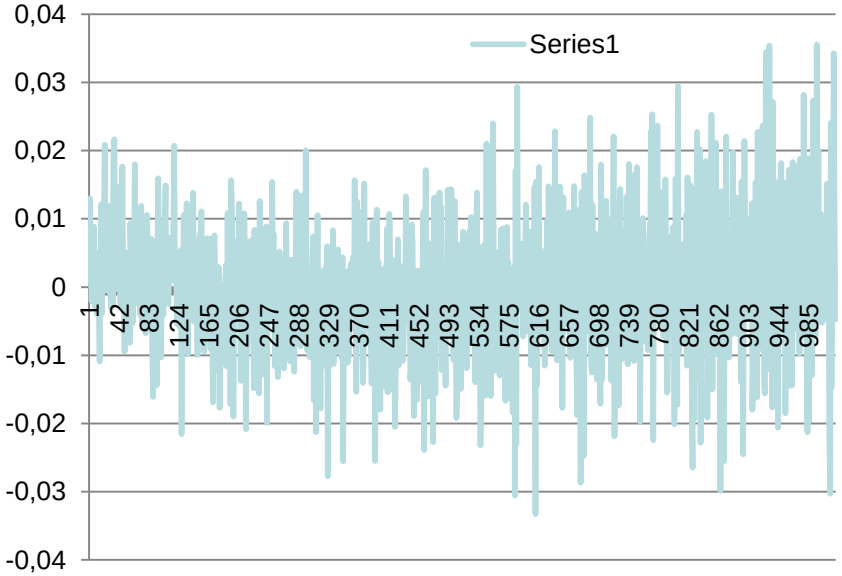
Digital domain	
System level protocol	2 – 200 Mbit/s Space Wire **Passed @ room temerature**
ROIC digital control	32 **Passed @ room temerature**
ROIC monitoring and trigger inputs	8 **Passed @ room temerature**
ROIC programming channel	1 SPI **Passed @ room temerature**
SRAM	**Passed @ room temperature**

Tests results

REQUIREMENT/ SPECIFICATION	TEMP.	RESULT
Regulator low supply voltage	RT	3.6V
ROIC supply noise	RT	150-200 uVrms
ROIC current	RT	50mA
ROIC supply output impedance	RT	≤0.5 Ohm
Power supply rejection ratio	RT	≥42dB
Temperature sensor	10-40°C	2mV/K
Bandgap Voltage	10-40°C	1,350V

10bits dac INL /DNL rail to rail





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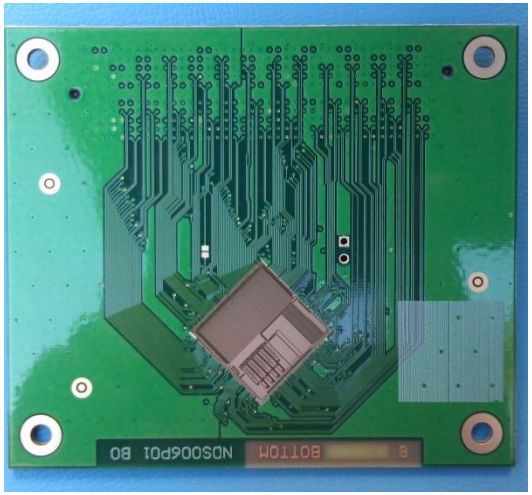

Conclusions

- Custom design high performance mixed signal ASIC
- From cryogenic (77K) to room temperature
- Radiation hard for TD and SE
- Highly flexible for ROICs
  - Highly programmable sequencer
  - Wide programmability and large dynamic ranges in analog circuits
- Beyond IR imagers

Next steps ?

- More Testing!
- More discussion with instrument builders and IR sensor manufacturers for further enhancements
- Larger Asic with multiple channels (32)
- Faster ADCs are under development (up to 12MSamples /s with reduced resolution)
- Irradiation testing and deeper temperature testing

Thank you!