caeleste

Scientific Detector Workshop
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Driving, conditioning and signal acquisition Prototype ASIC for Large Format NIR/SWIR Detector Array

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A Finmeccanica Company

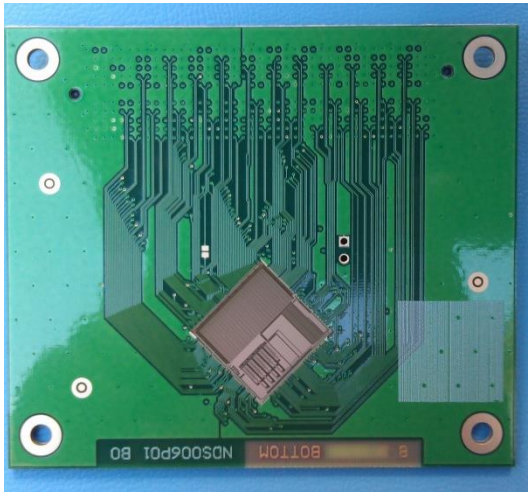
esa

easics

status

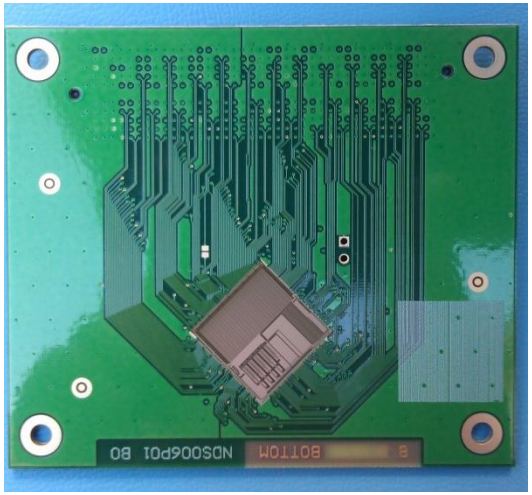
- **Development in two phases:**
  - Prototype ASIC (2013)
  - Final product design (2014-2015)

  - Device is just back from foundry:
  - Tests will go on until jan 2014



Outline

- **Motivation and technical challenges**
- **Design for Radiation hardness and Cryogenic temperature**
- **Circuit design and simulation**
- **Test setup**
- **Conclusions**



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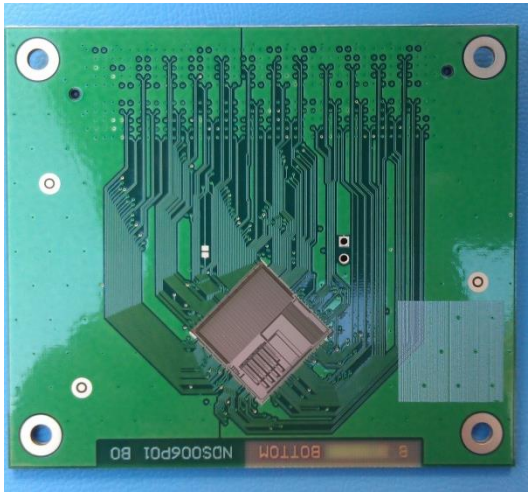


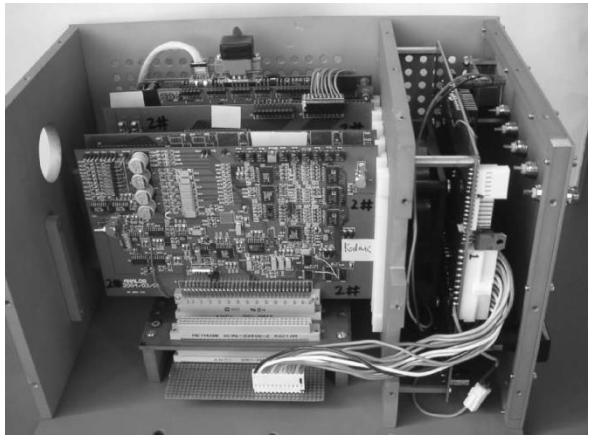
A signal conditionning ASIC

This development aims at providing the community with a signal conditioning ASIC

- **Tailored to imagers (especially IR sensor)**
- **Versatile**
- **With a wide operating temperature range**
- **Taking in consideration multiple IR detector manufacturers specificities**
- **Able to drive multi-sensor systems**

Why an ASIC ?

Data acquisition and control system for IR imagers



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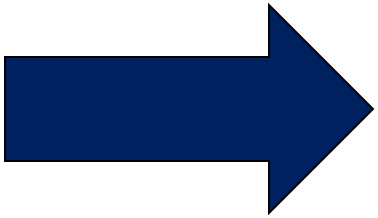
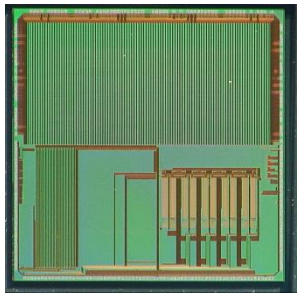




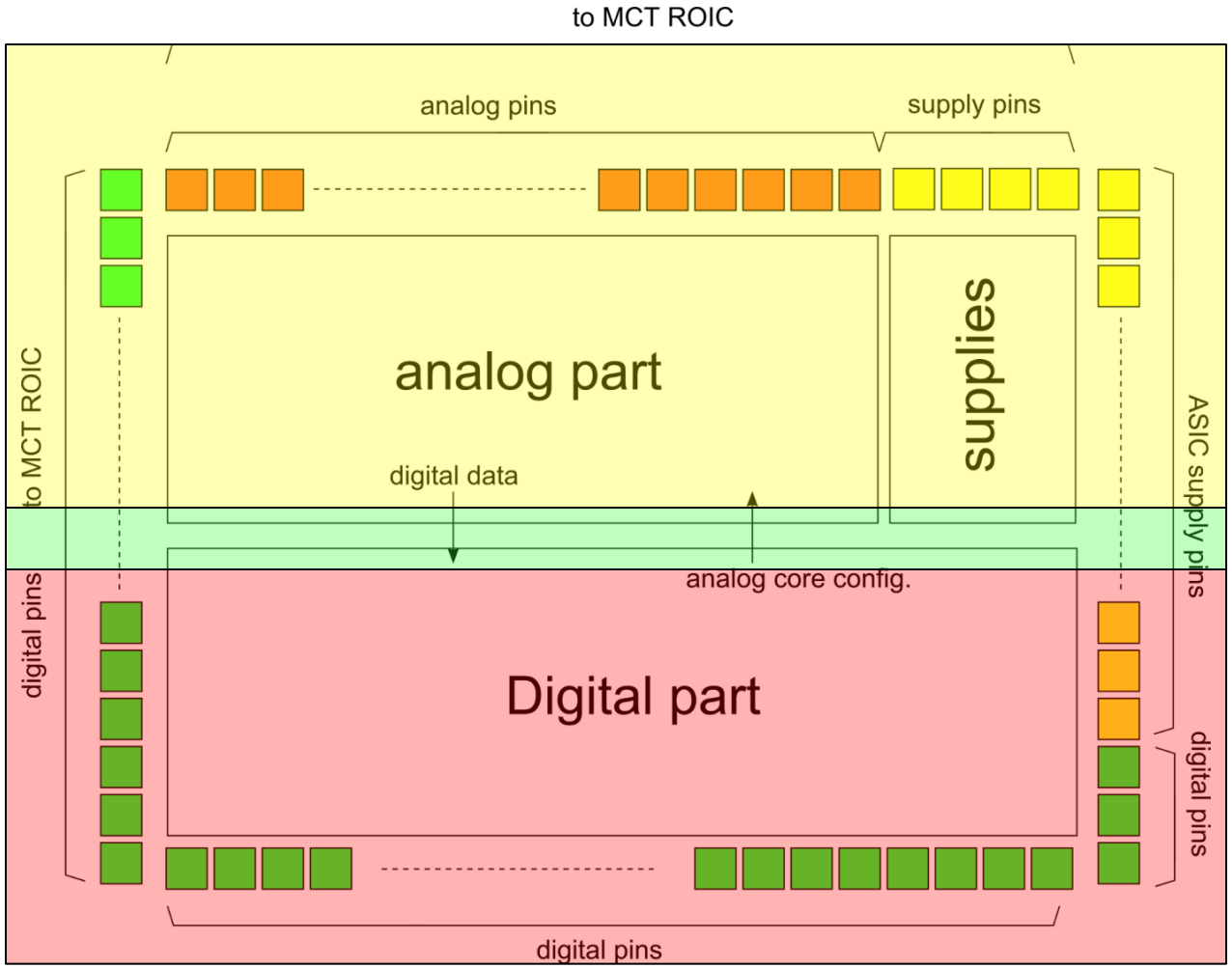
Analog domain

- Signal conditioning
- Analog to digital converter
- Regulated power supply
- Bias voltage/current references

Digital domain

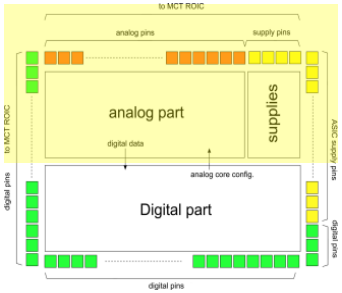
- Digital control core
- Memory & Clock
- Data Communication

A true mixed mode ASIC



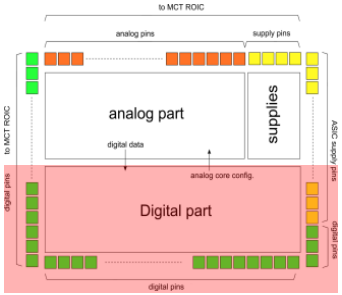
Challenging specifications

Analog domain		
Function	**No.**	**specifications**
LDO	4	1.3-3.4 [V], 100mA max. supply current
Analog inputs	16	
Preamplifier / CDS / Offset cancellation	4	5 gains, 25uV RMS noise 8 bits Offset removal
16-bit ADC	4	Successive approximation with bits calibration Target DNL < 1,5 LSB
ROIC bias and Reference voltages	16	10 bits, rail to rail operation
ROIC health monitoring	4	Resistors / differential voltage monitoring 16 bits
Internal reference	1	1.2V Bandgap
Temperature sensor	1	



Challenging specifications

Digital domain	
Master clock	0 – 200 MHz
System level protocol	2 – 200 Mbit/s Space Wire
ROIC digital control	32
Scheduler time granularity	10M updates/s
Sequence nesting depth	8
ROIC monitoring and trigger inputs	8
ROIC programming channel	1 SPI



Environmental constraints

Challenging design for:

- **Cryogenic temperature (77K)**
- **… but not only: operates from 77K to room temperature**
- **Radiation tolerance in space (designed up to 1Mrad TID, 60MeVcm^2 /mg SEU)**
- **High reliability**
- **Scalalibility**

Outline

- Motivation and technical challenges
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Radiation hardness

Radiation hardness is a concern for:

- Synthetized digital logic
- Analog custom designed cells

Radiation hardness: digital design

The project uses DARE Library

- Developed by IMEC
- Designed up to Mrad, used in flight models
- DARE180 (UMC 0.18um 1P6M CMOS)
- Radiation Hard Standard Cells, SRAM, I/O cells, PLL
- Intrinsic protection against Latch up and TID
- Flip-flop protected against SEU
- Allows custom mixed-signal design

Radiation hardness: digital design

Beyond library, circuit topology is rad hard:

- Redundancy
  - Hamming Codes
  - Parity check
  - Safe FSMs
- Watchdog Timers

Radiation hardness: analog design

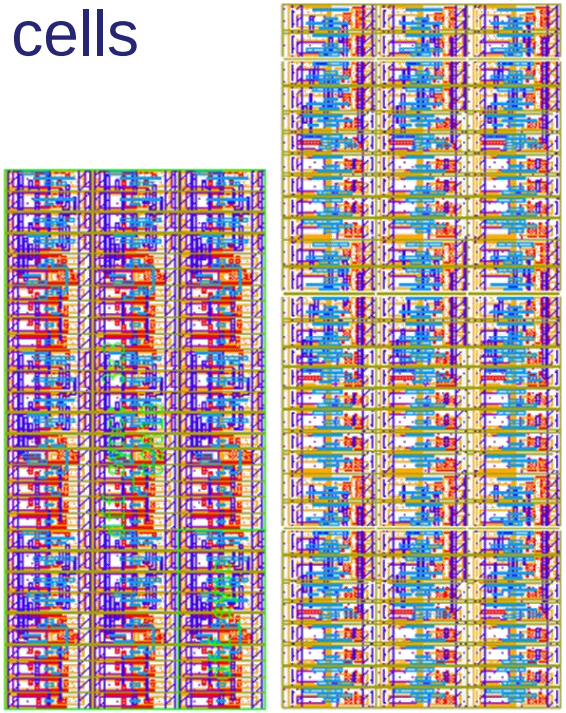
DARE has a limited subset of analog component.

Caeleste uses its own radhard cells

- Analog and High Voltage logic standard cells
- Full custom tactical cells

Prevention for:

- Single Event
- Total dose



Layout using Caeleste's standard library (left) and the same in the fully radiation hard library (right)

Design for low temperature

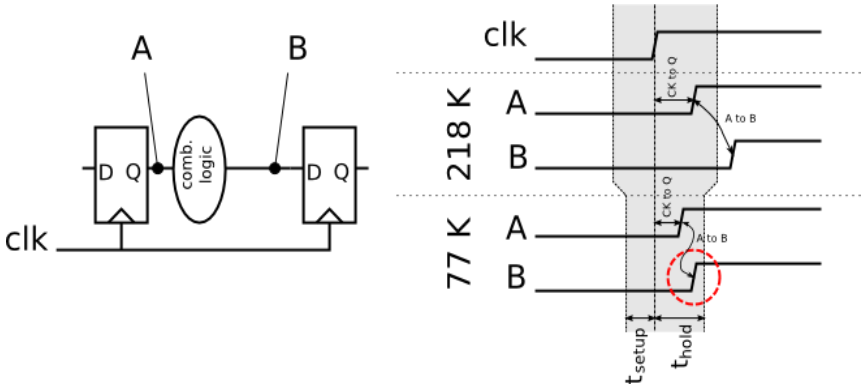
Analog and digital flow require different approach on modeling and design strategy for cryogenic temperature:

- Synthetized digital logic:
  - Validation of key blocks (such as SRAM)
  - A derating of speed, power, etc. of the library
- Analog custom design:
  - Active and passive component

Cryogenic digital design

The DARE library has never been used at 77K

The logic becomes faster. However one must take care of set-up and hold time violation.

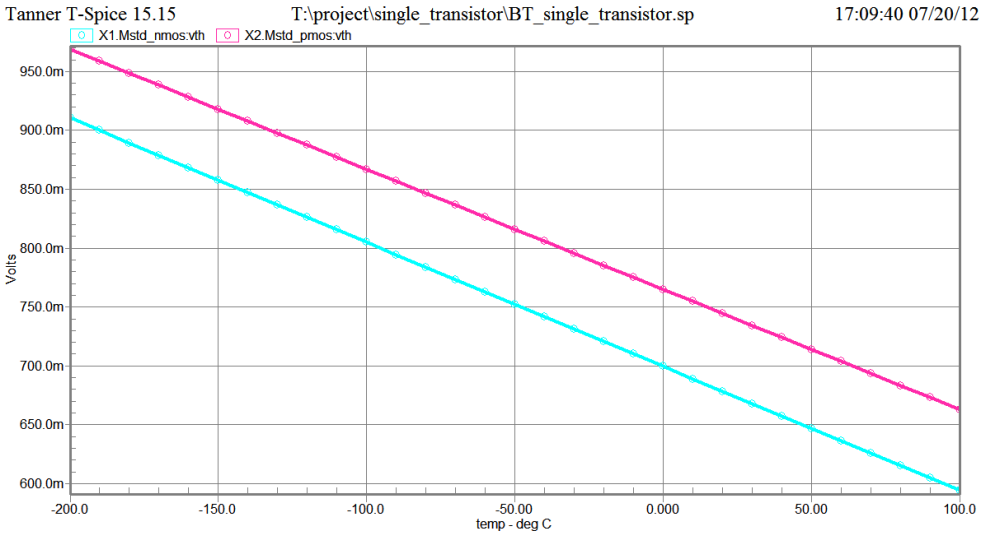


The library models have be adapted, based on a model characterized at 218K

Other components like SRAM are also to be validated still

Cryogenic analog design

- MOSFET modeling
  - V_{th}: increase
  - Mobility: increase
  - MOS switch: low R_{on}



- Careful choice of passive components
  - Highly doped non silicide poly Resistor for stability
  - MIM capacitors

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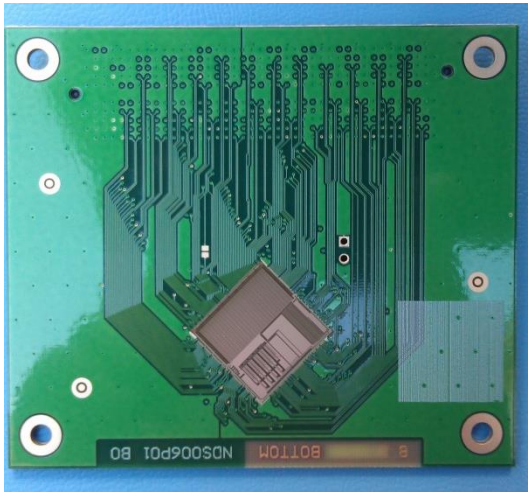
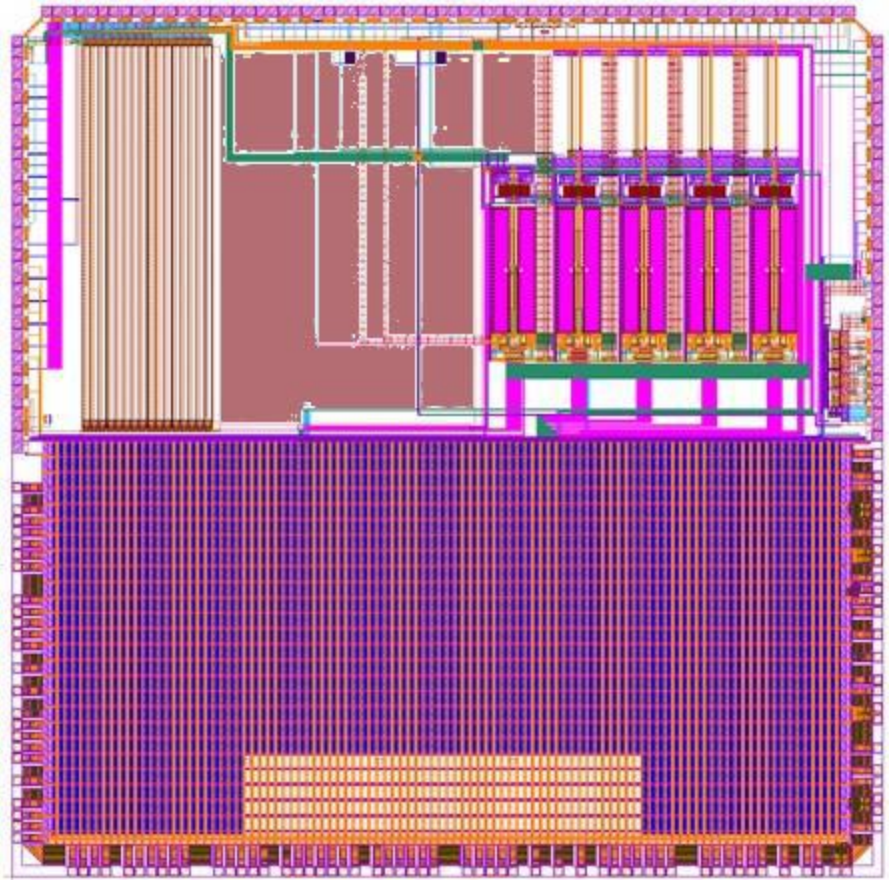
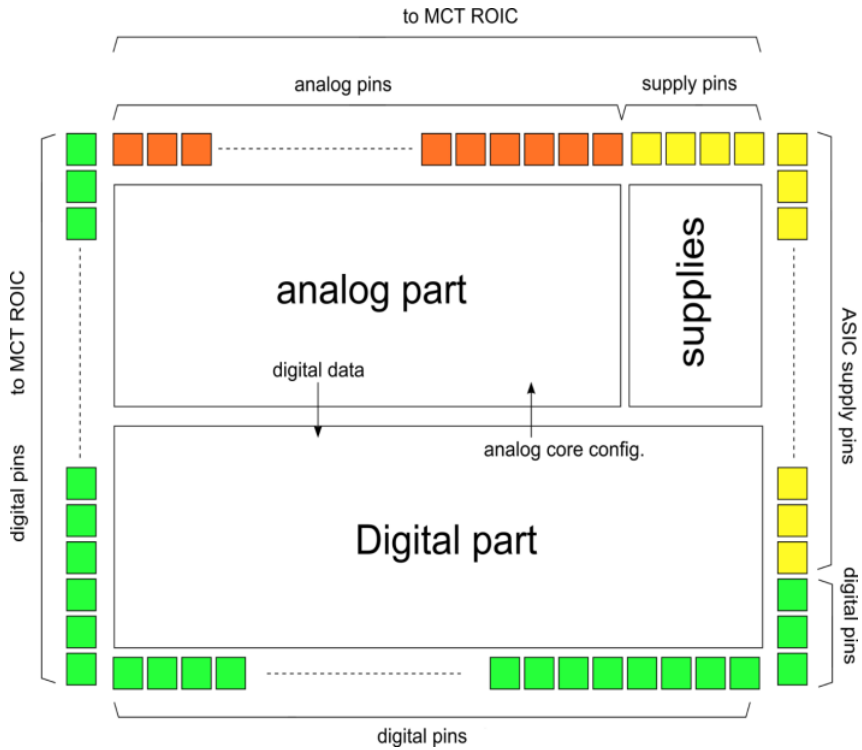


Analog section





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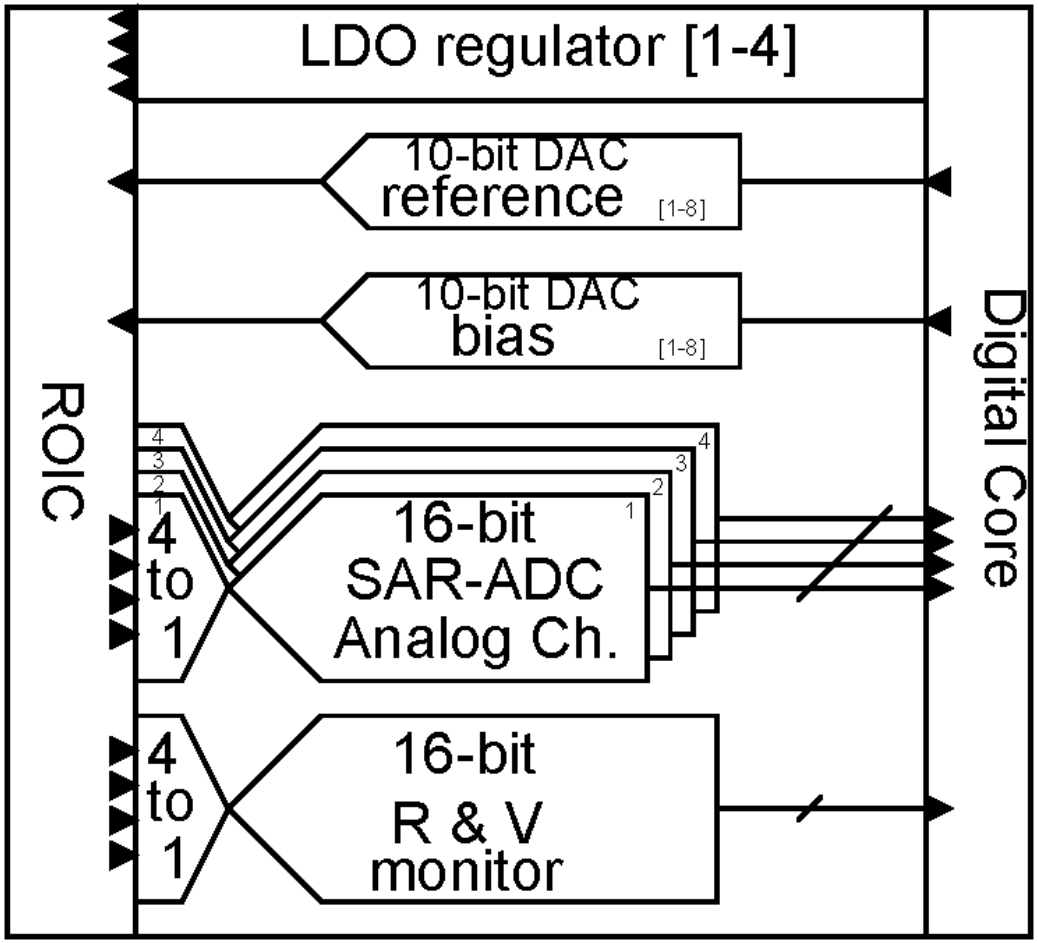
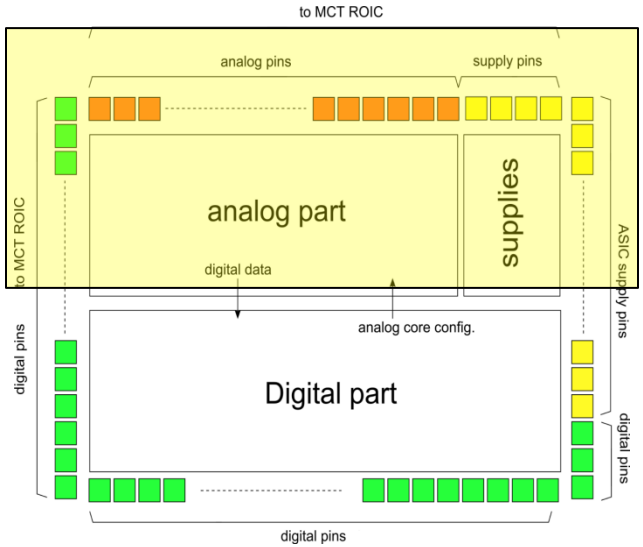
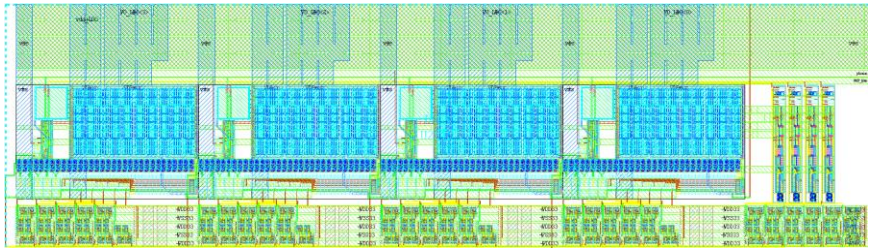


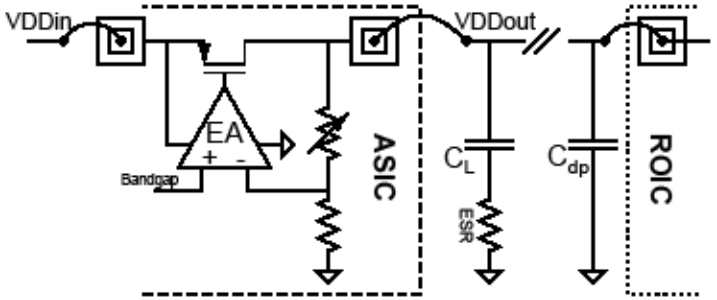


LDO

- LDO
  - Programmable output
  - Stability: PM>60°
  - Output current 0-100mA



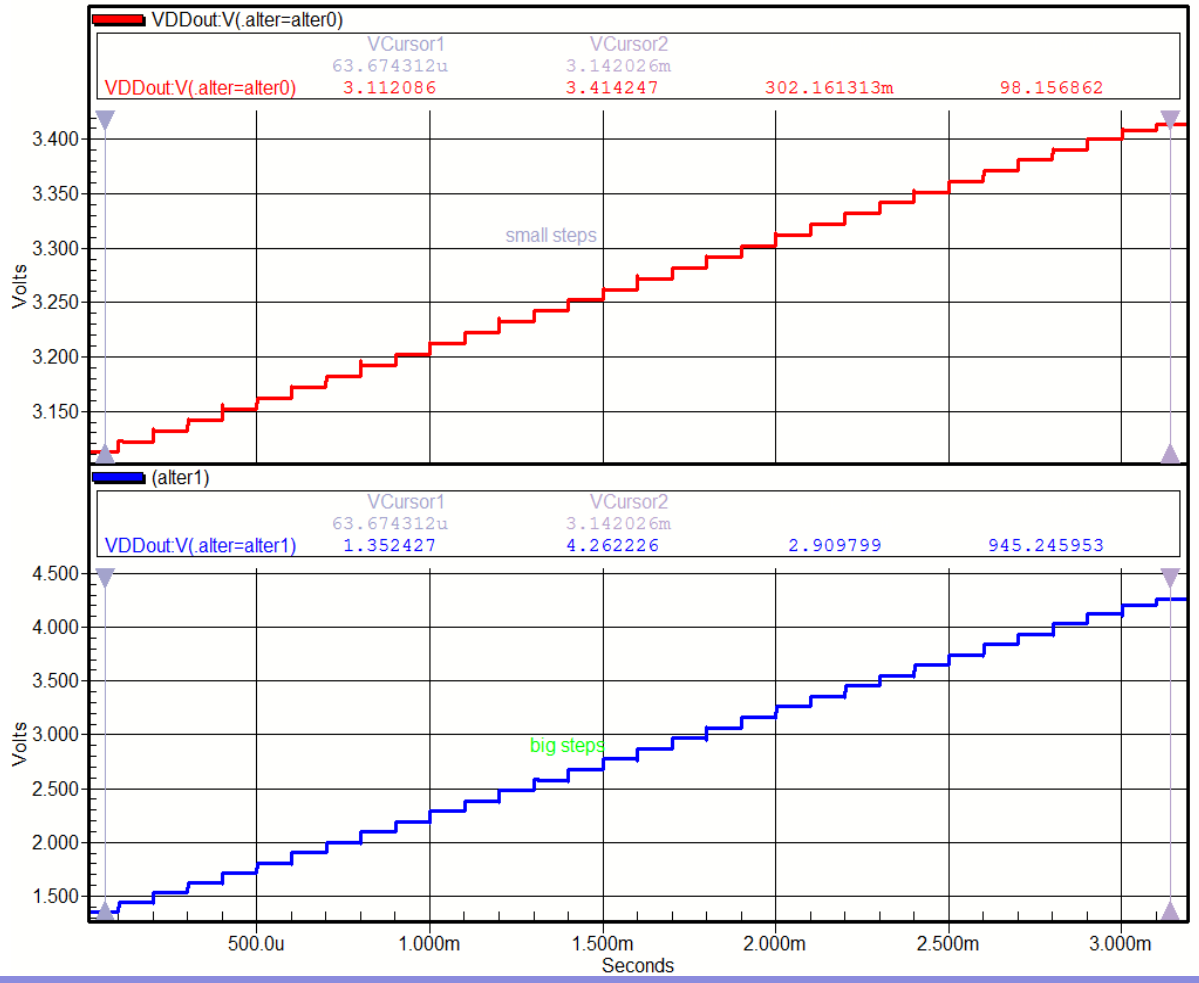
- Bandgap
  - 1.2V
  - 77K-300K



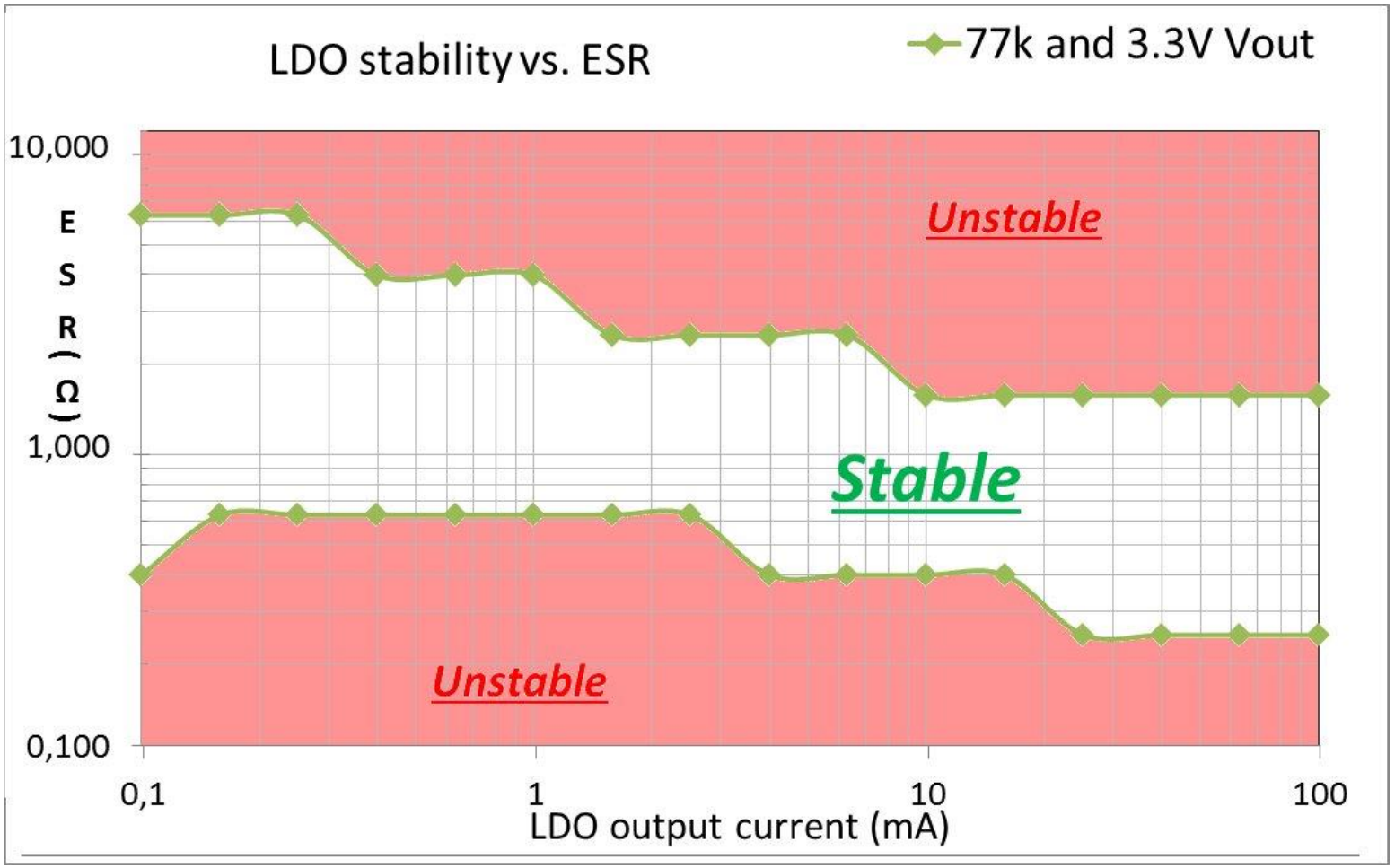
LDO: tunning range

Fine / coarse Tuning

Extended Range: 1,3…4,2V

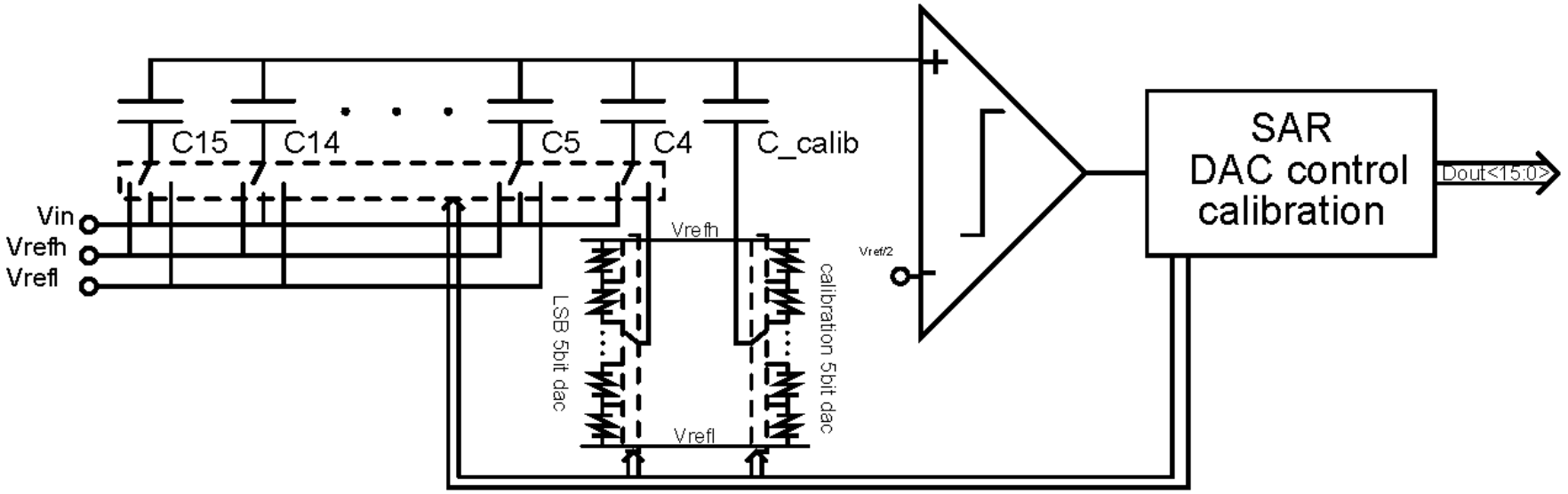


LDO: stability

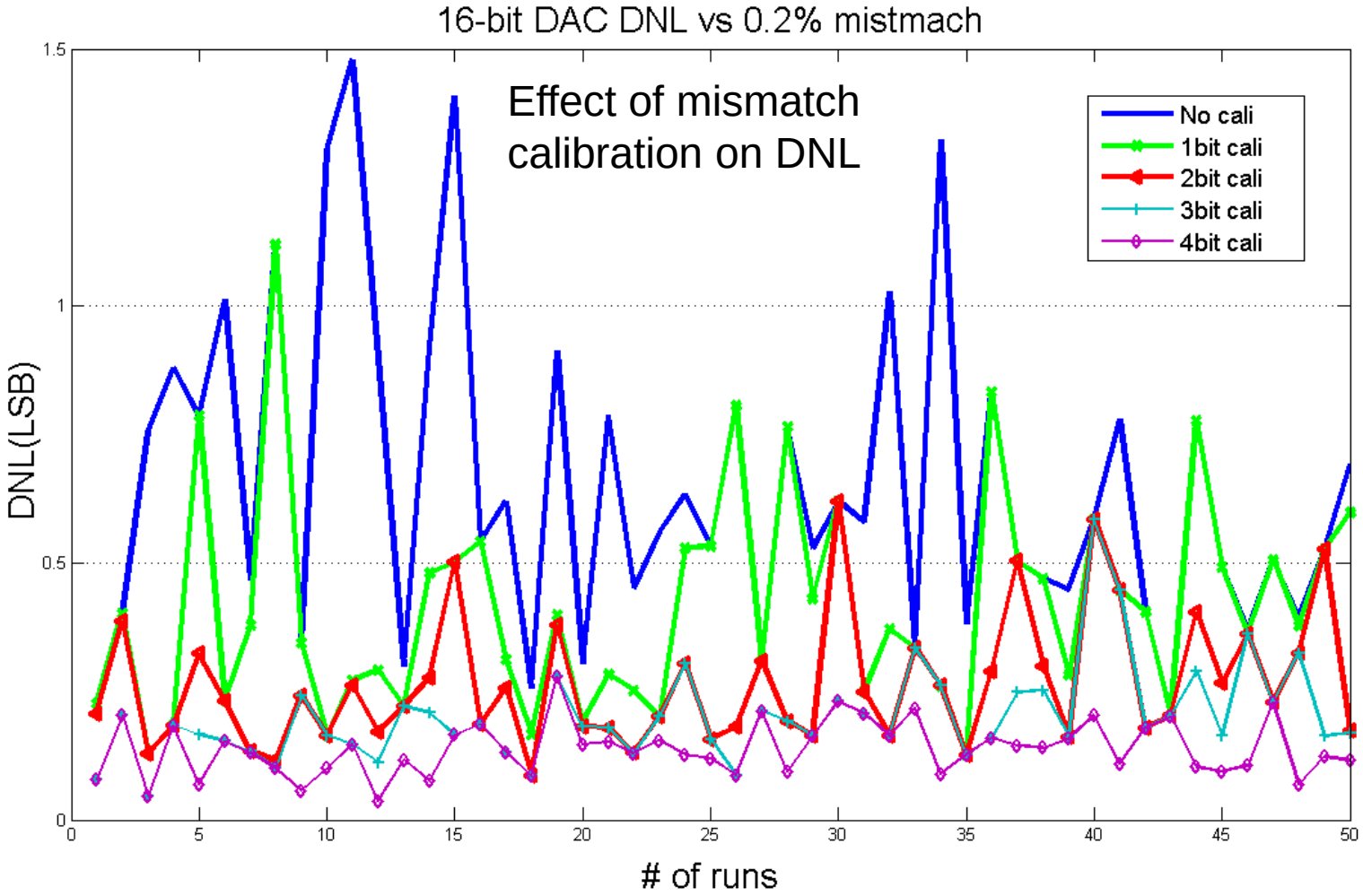


ADC

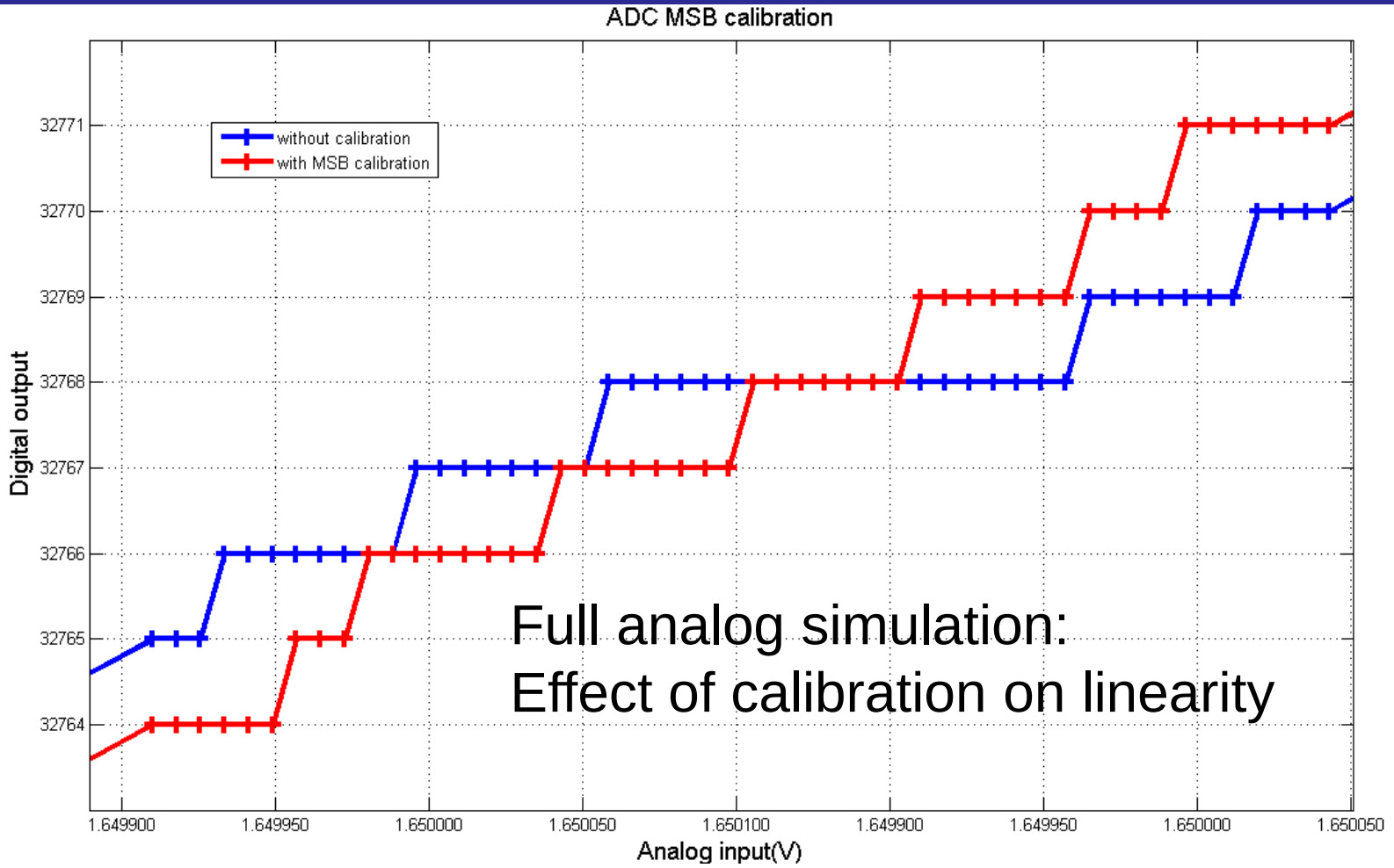
- 16-bit, 50-200kHz, fully differential SAR ADC
  - Feedback DAC 11 MSBs capacitive and 5 LSBs resistive
  - Low offset comparator: auto zero
- A calibration scheme is available



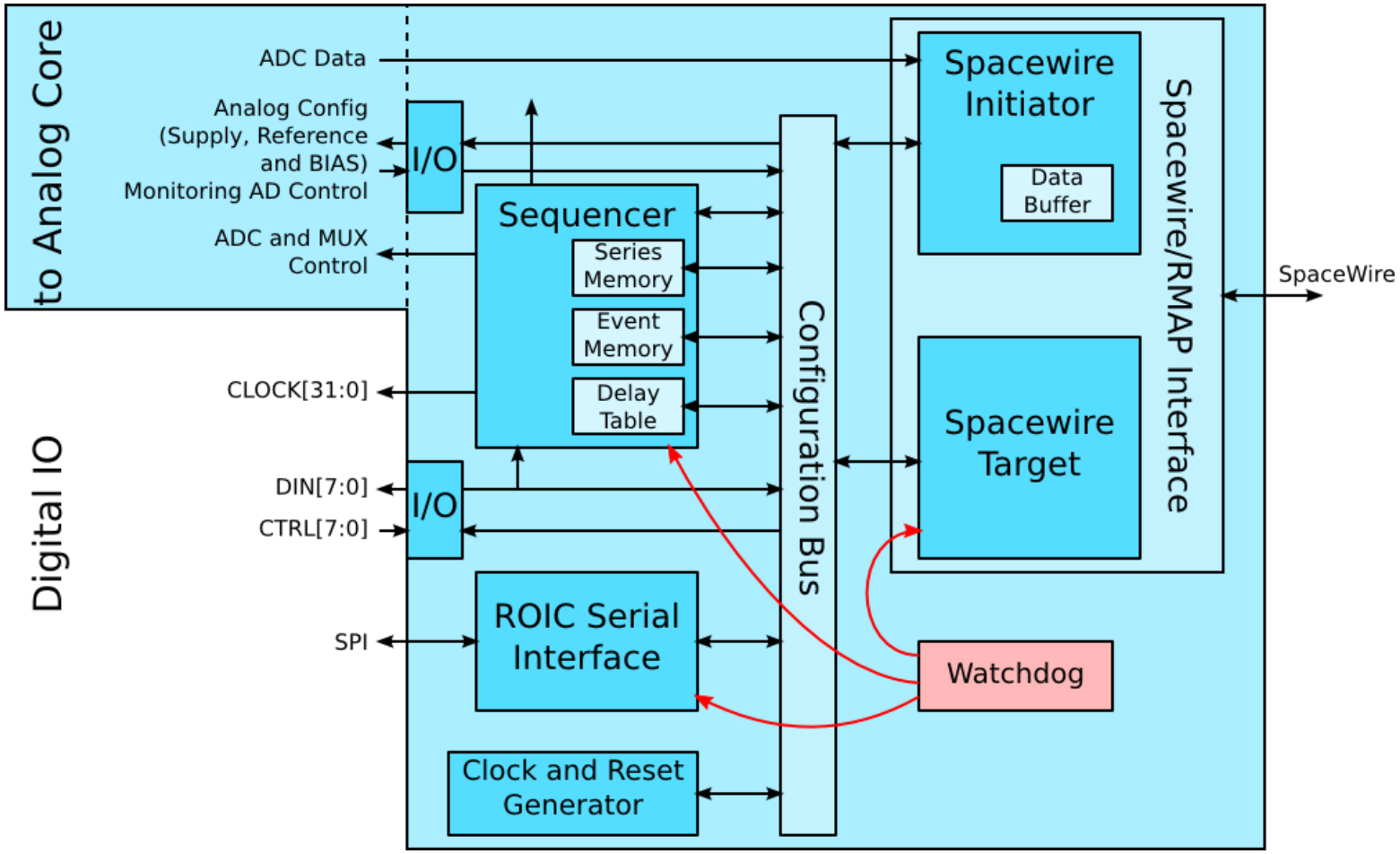
ADC: model driven design



ADC: design verification

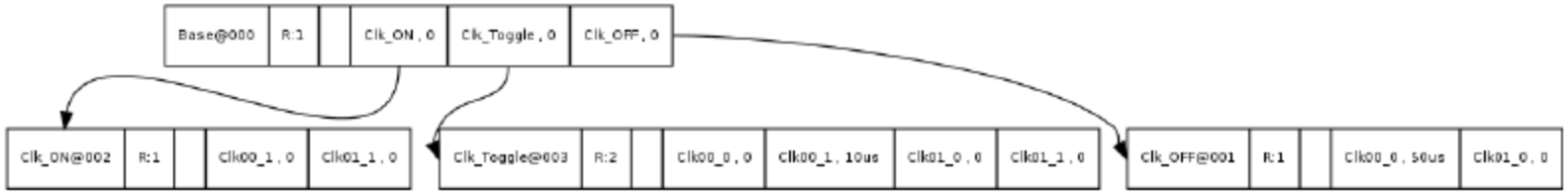


Digital design



Digital design

```
### Series Table
##########                    Repeat   Addr
#################################################################################
S Base                                 1     0
T       0          Clk_ON
T       0          Clk_Toggle
T       0          Clk_OFF
S Clk_ON 1
T       0          Clk00_1
T       0          Clk01_1
S Clk_Toggle2
T       0          Clk00_0
T    10us          Clk00_1
T       0          Clk01_0
T       0          Clk01_1
S Clk_OFF1
T    50us          Clk00_0
T       0          Clk01_0
```



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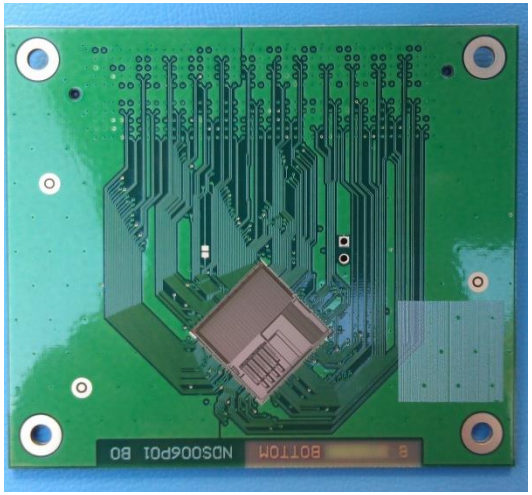

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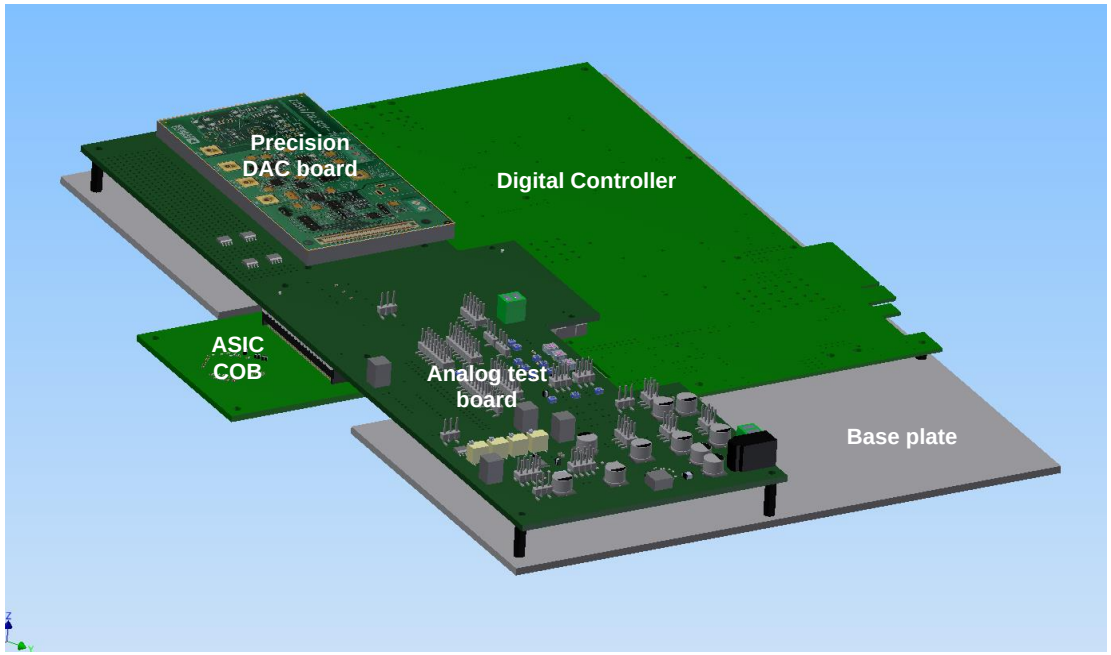

Unified design for:
Room temperature board
Cryogenic temperature

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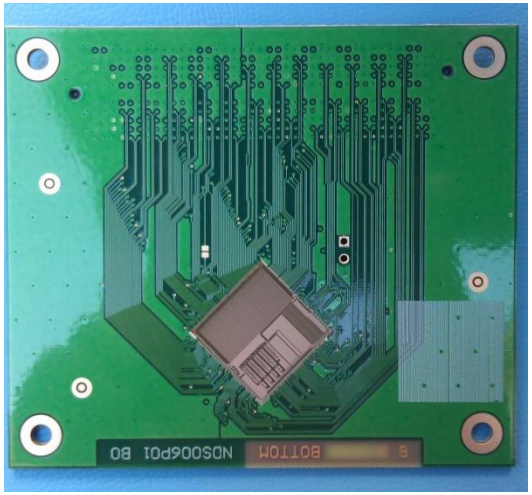

Conclusions

- Fully custom design high performance mixed signal ASIC
- From cryogenic(77K) to room temperature
- Radiation hard for TD and SE
- Highly flexible for ROICs
  - Highly programmable sequencer
  - Wide programmability and large dynamic ranges in analog circuits
- Beyond IR imagers

Next steps ?

- Testing!
- Larger Asic with multiple channels (32 to 64)
- Faster ADCs are under development (up to 12MSamples /s with reduced resolution)
- More discussion with instrument builders and IR sensor manufacturers for further enhancements
- Irradiation testing and deeper temperature testing

Thank you!