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Fast Charge Transfer in 100µm long PPD Pixels

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Abstract

We present a photodiode structure for fast charge transfer in narrow and elongated pixels. For applications requiring high frame rate and elongated pixels, charge diffusion in photodiode limits the transfer efficiency (transfer time < 1µs). We solve this by creating an electrostatic potential gradient in the direction of transfer by exploiting the proximity effect of implanted regions on the pinning voltage. The proposed method is realized in a pixel with dimension of 7 µm x 100 µm. The method does not influence the quantum efficiency and uses a standard 0.18 CIS process.

Introduction

PPD design methods have been proposed in the literature to reduce the diffusion time by creating an electrostatic potential gradient in the PPD. The methods employ the fact that the pinning voltage of the PPD is influenced by one or a combination of the below mentioned conditions.

1. Shape of the PPD implant [1,2,3,4]
2. Dose of the PPD implant [3]
3. Dose of pinning layer over the PPD implant or multiple epitaxial substrates [5]

Design Methods	Drawback
Shape of PPD implant	Lower sensitivity near narrow PPD width
Dose of PPD implant	Process modifications
Dose of pinning layer over PPD or multiple epitaxial substrates	Process modifications

PPD Concept

The pinning voltage of a photodiode is influenced by the proximity of another implanted region. In this work, a standard P+ implant is used to influence the pinning voltage as shown in Figure 1. The Pinning voltage of PPD vs the gap between P+ implant and PPD is shown in Figure 2.

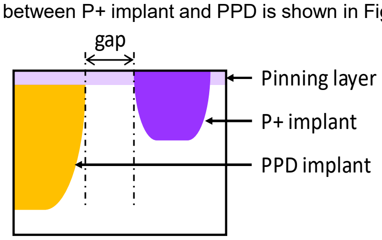

Figure 1: Cross-section view of PPD with P+ implant

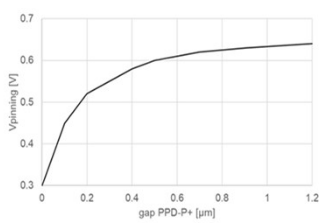

Figure 2: Pinning voltage of PPD vs the gap between P+ and PPD

TCAD Simulations

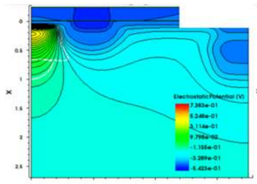

Figure 3: Gap = 0 µm

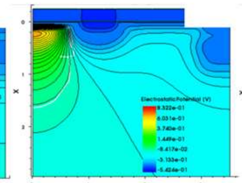

Figure 4: Gap = 0 µm

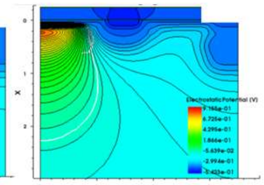

Figure 5: Gap = 0 µm

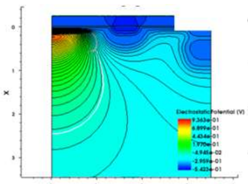

Figure 6: Gap = 0.7 µm

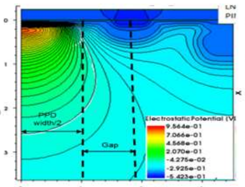

Figure 7: Gap = 0.9 µm

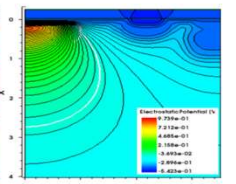

Figure 8: Gap = 1.2 µm

In Figure 3 the depletion region is restricted to a very small area when P+ implant touches PPD. As the gap increases from Figure 4 to Figure 8 the depletion region is extended deeper and wider into the bulk silicon.

PPD Structure

The gap between P+ and PPD implant is changed along the direction of charge transfer from PPD to FD such that a constant electrostatic potential gradient is created. The potential gradient will ensure that charges undergo drift instead of diffusion. The resulting layout is shown in Figure 9.

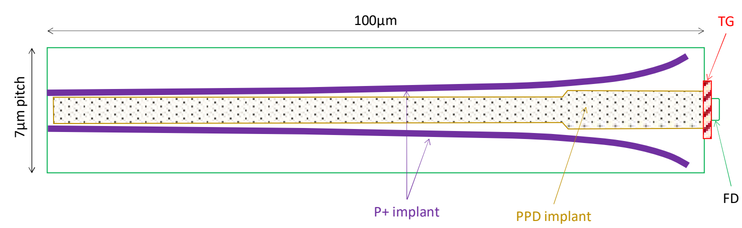

Figure 9: Pinning voltage of PPD vs the gap between P+ and PPD

Measurement Results

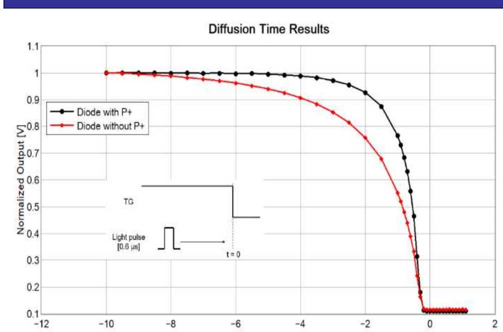

Figure 10: Diode with and without P+ implant

The position of the light pulse (width=0.6 µs) is moved closer to the falling edge of the TG (t=0) for each measurement point. It can be observed that the potential gradient in the diode with P+ results in faster charge transfer compared to the diode without P+.

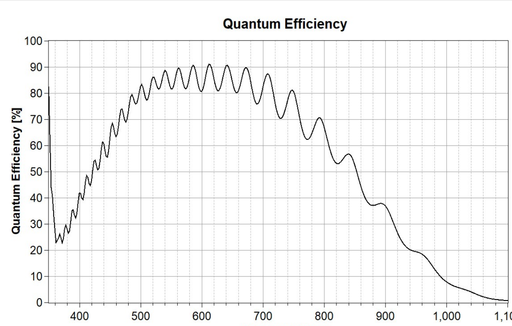

Figure 11: QE of diode with P+ implant

The shape and layout style does not influence the overall sensitivity of the diode as can be concluded from the quantum efficiency (QE) results.

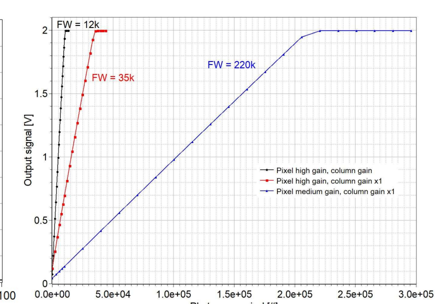

Figure 12: Photo response for different pixel gains

The charge handling capacity of the diode is not influence by using P+ implant

References

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