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Backside thinned, 2.5 e^-_{RMS}, BSI, 700fps, 1760x1760 pixels wave-front imager with 88 parallel LVDS output channels

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Introduction: from application to image sensor challenges

The image quality of ground-bases telescopes is limited by atmospheric turbulence. In order to achieve diffraction limited imaging performance in the next generation giant telescopes, it is necessary to track the effect of atmospheric turbulence, which is seen as a disturbance the optical wave-front, at a millisecond time scale at a fine grained spatial resolution. This is done by recording the image of a laser guide star (LGS) or a bright natural guide star (NGS), for each of the deformable mirror segments at high frame rate. The image is then processed and used to steer the array of deformable mirrors to correct the image in real-time [1-2]. The image sensor array has 88x88 "sub-arrays" of 20x20 pixels, each sub-array corresponding to one such deformable mirror segment. The 1760x1760 pixel imager, operates at nominally 700 (up to 1000) fps, which is equivalent to a sustained pixel rate of ~3 Gpixel/s or ~30Gb/s. Pixels will be backside illuminated to reach 90% QE, have less than 3 noise electrons including the ADC. The high pixel rate forces to read out the digital data over 88 parallel LVDS channels at 210 up to 420 Mb/s.

An important set of challenges is related to the huge digital parallelism, and the 88 parallel LVDS ports. A specific issue is the clock distribution network that enables synchronous operation of these 88 LVDS channels.

Image sensor specifications

Two generations of the sensor will be built. The actual 1st generation quarter device is called NGSD (natural guide star detector), and is a 880x840 pixel array. The subsequent LGSD (laser guide star array) is a 1760x1760 pixels imager.

A small area (60x60 pixels) "TVP" technology validation demonstrator has been built and evaluated to prove key performance. It has the same pixel as the NGSD and LGSD, the full analog circuit chain including the ADCs. The TVP allowed validating electro-optical performance as front side QE, noise, linearity, image lag, charge conversion factor, and ADC timing. From the TVP to the NGSD the essential new challenges are all related to the size, the long supply and signal distribution networks, clock and signal skew, and digital to analog crosstalk.

Image sensor specifications are shown in next table.

Pixel array (including dark reference pixels)	Stitched design for two versions: 880x840 pixels ("NGSD") or 1760x1760 pixels ("LGSD")
Technology	backside thinned CMOS 0.18µm
Pixel pitch	24µm
Pixel topology	4T pinned photodiode pixel
Array architecture	1680x1680 pixels organized in 84x84 time coherent "sub arrays" of 20x20 pixels, with a total LGSD image size of 4x4cm
Shutter	Rolling shutter in chunks of 20 rows, so that within a sub-array (20 rows x 20 columns) detection is synchronous.
Responsivity	100 to 160 µV/electron in TVP pixel variants
Pixel full well Q_{FW}	4000 e- (on TVP)
Read noise including ADC	$2.5e^-_{RMS}$ (on TVP)
Number of rows read in parallel	40 (LGSD) or 20 (NGSD) rows over 20 parallel column lines per column of pixels
Number of ADC's	40x1760 (LGSD) or 20x880 (NGSD)
Number of parallel LVDS channels	22 (NGSD) or 88 (LGSD)

LVDS channel bit rate	210 Mb/s baseline, up to 420 Mb/s
QE	QE above 90%, for 24x24µm, backside illuminated (BSI) pixels over the visible range *or* optimized for the wavelength of the laser guide star.
Image lag	<0.1 % (TVP)
MTF	Near ideal and symmetric in X and Y by design
Frame rate	between 700 and 1000fps, reading 2 to 3 Gpixel/s or 20 to 30 Gb/s over 88 parallel LVDS channels
Power dissipation	Maximum 5W overall, including the 88 LVDS drivers
LVDS driver dissipation per channel	6.0 mW @ at maximum data rate. 4.5 mW in sub-LVDS

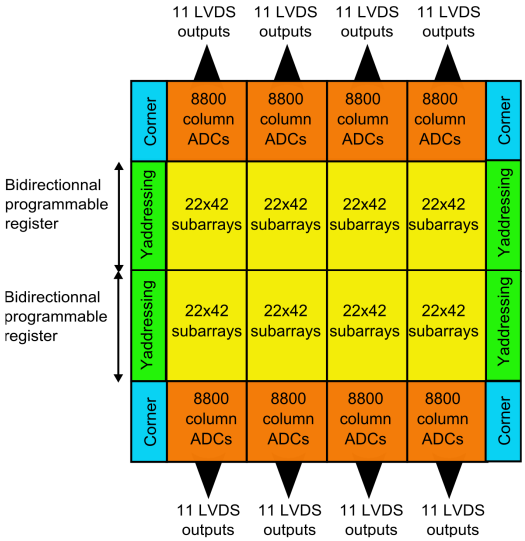

Figure 1: LGSD top-level floor plan composed of stitch blocks

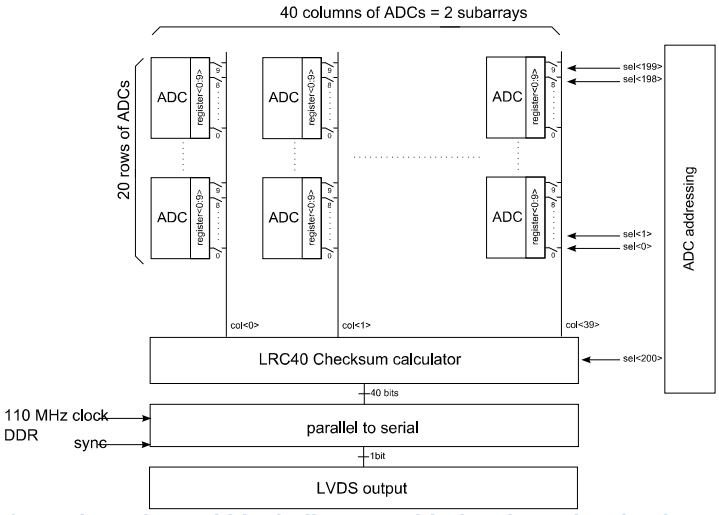

Figure 2: readout channel block diagram with data integrity checksum block

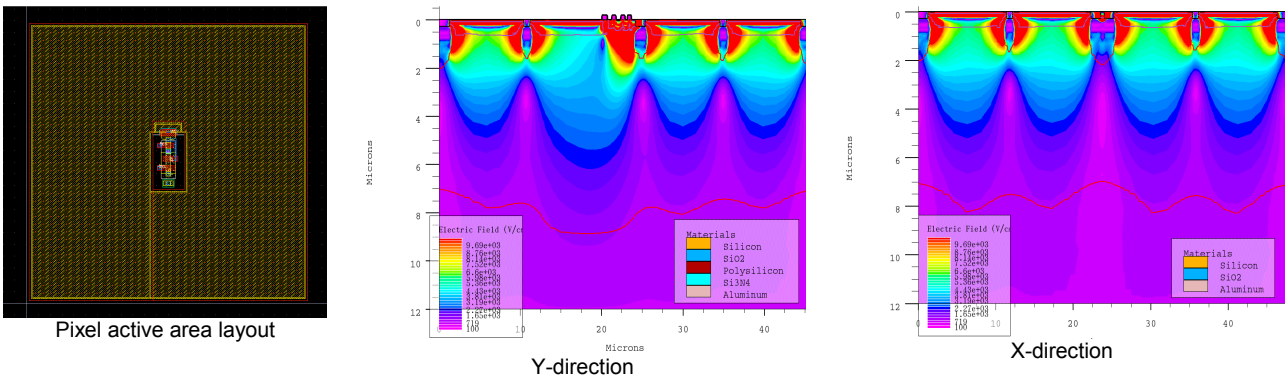

Figure 3: pixel design for best centroiding performances, TCAD simulations

Low skew clock distribution network.

Creating a common clock and synchronization for 88 LVDS drivers that are dispersed over two lines of 4.5 cm is a challenge. A specified 300 ps clock and sync skew cannot be reached by a single nor by a two-sided input signal. The classic approach to make a symmetrical clock tree is not feasible in case of a stitched, thus repetitive, layout.

Our approach tries to solve the constraint of repetitivity by the programmability of each repeated block. From basic simulations, we know that a 2 level clock tree as in Figure 4 has low enough skew for the specifications. Figure 5 is a close approximation based on repetitive programmable blocks. Simulations show that this scheme has a maximum skew of about 150ps in TT process conditions.

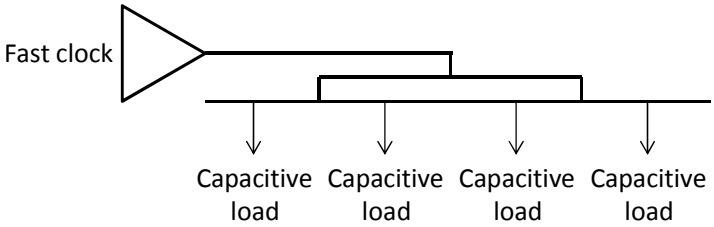

Figure 4 symmetrical clock tree with 2 levels, of wich the lowest level is shunted to become one continuous clock line.

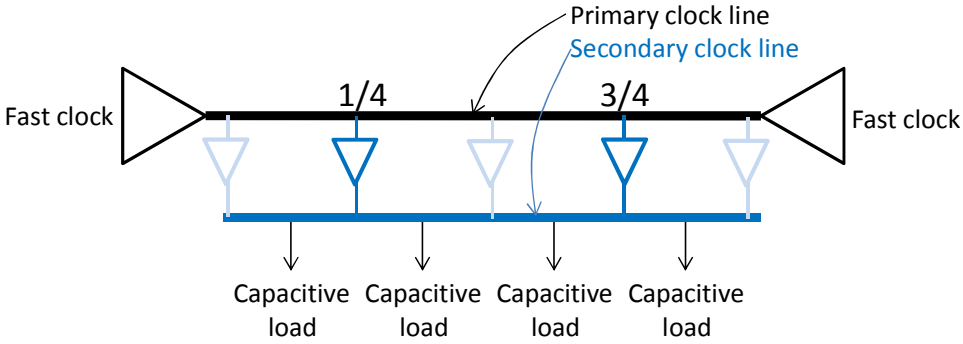

Figure 5 concepts of a programmable 2-level clock distribution scheme. Buffers from primary to secondary clock lines are equally distributed along the lines, but only the buffers at positions ¼ and ¾ are activated.

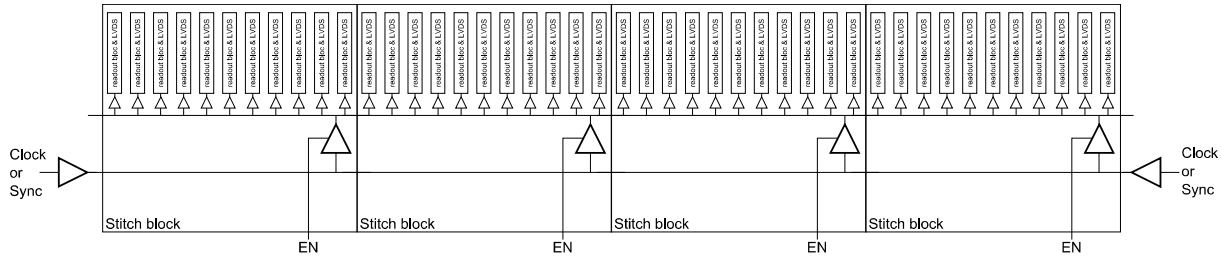

Figure 6: practical implementation of the programmable low skew clock distribution scheme. "EN" enable bits are stored via an SPI channel.

References

[1] M. Downing & al, "AO Wavefront Sensing Detector Developments at ESO", SPIE proceedings 7742, June 2010

[2] http://www.eso.org/sci/meetings/dfa2009/Presentations/Downing_A0WFS_DfA2009-3.ppt

[3] J. Pratlong, A. Defernez, B. Dierickx, B. Dupont, P. Jerram, P. Jorden, A. Walker, A. Pike, M. Fryer, "Low Noise, high speed, high QE CMOS image sensor", CNES Workshop, 8-9 Dec 2009, Toulouse