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Round Table on
Nano CMOS and 3D electronics for Scientific Instrumentation and Imaging:
Opportunities and practical aspects

Round table introduction slides

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Why do we need nano & 3D?

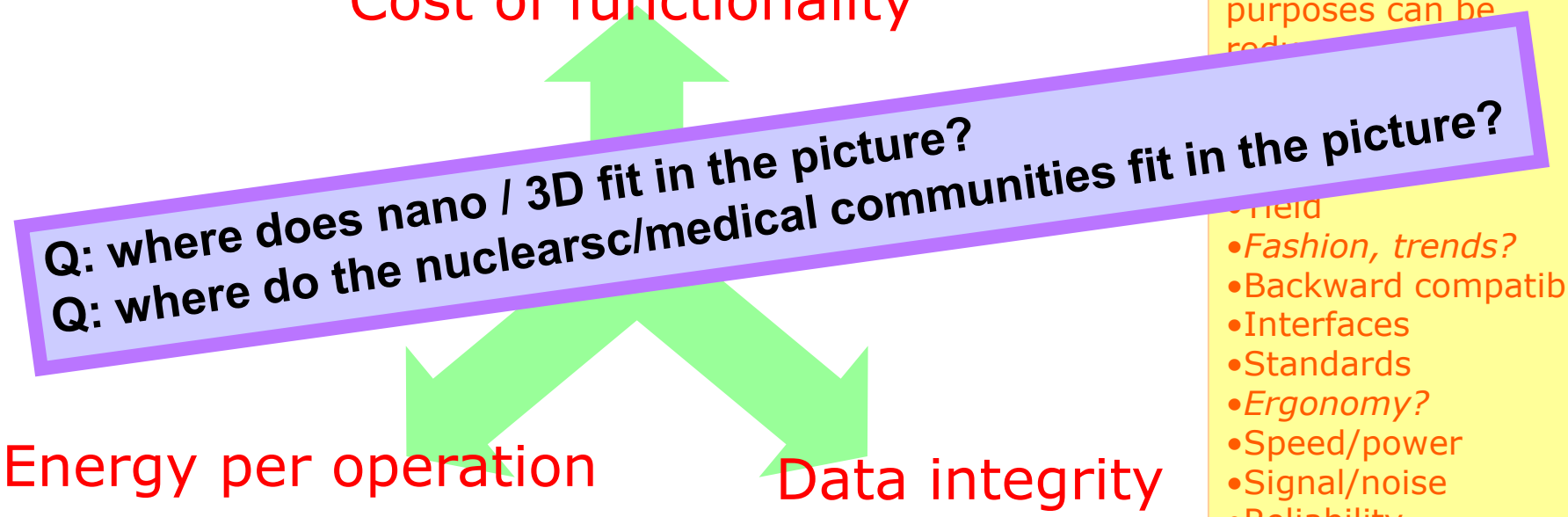
- Supply & demand situation

Demand:
•There are needs (don't ask me – you tell me! But it has something to do with)
→ Size
Macroscopical (array)
Pixel size
→ Data bottlenecks
speed, processing close to the signal source, integrity
→ Performance
noise, S/N, sensitivity
→ Cost

Supply:
•There happens to be a micro-electronics industry that has an enormous drive for "scaling"
•Supply is discriminatory
→Technology research caters ONLY to the very high volume markets
→ Other markets "may use as is" and use affordable modifications

Micro-electronics industry challenges triangle

The purpose of integration and scaling, and the associated challenges are:

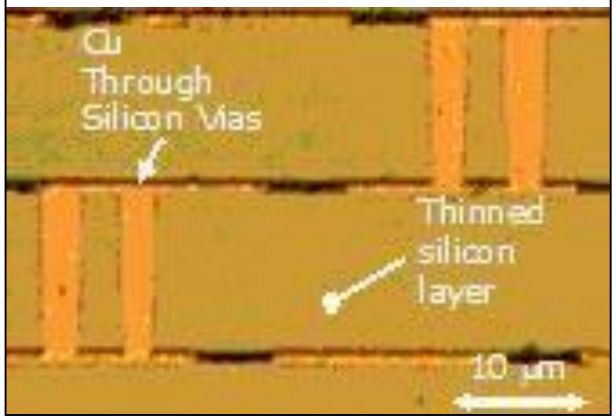


95% of all specs and purposes can be red…

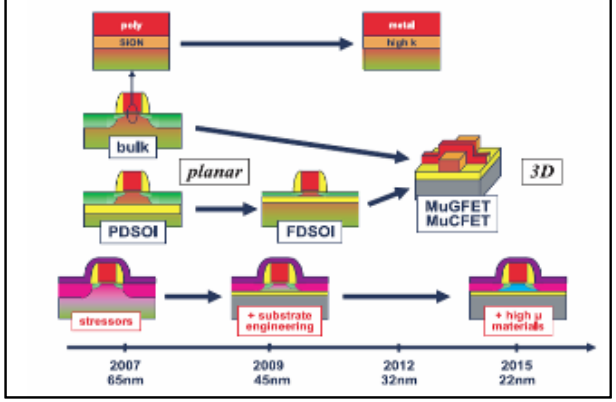
- Yield
- *Fashion, trends?*
- Backward compatible
- Interfaces
- Standards
- *Ergonomy?*
- Speed/power
- Signal/noise
- Reliability
- Confidentiality
- Operational lifetime
- Security
- …
- …

Trends in Manufacturing Technologies

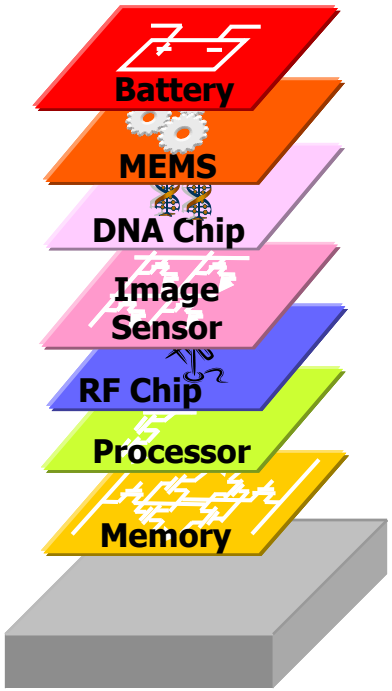
3D technologies



2D technologies



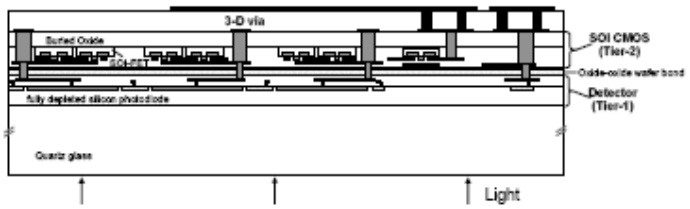
A wealth of opportunities, but also an explosion of degrees of freedom for design



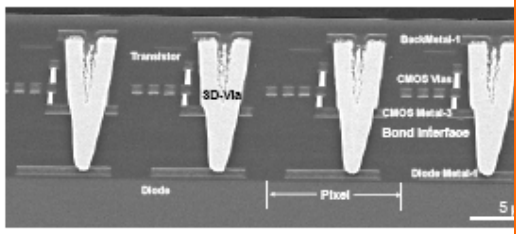
Courtesy P. Marchal IMEC 2008

3D? Yes there is significant progress

3D integration is driven by mainstream [SoC] industry
Spinouts to 2nd tier markets has potential



19.6.1: Schematic diagram of 3D stacked imager circuit. Tier-1 is a silicon photodetector wafer and Tier-2 is an inverted FDSOI CMOS wafer



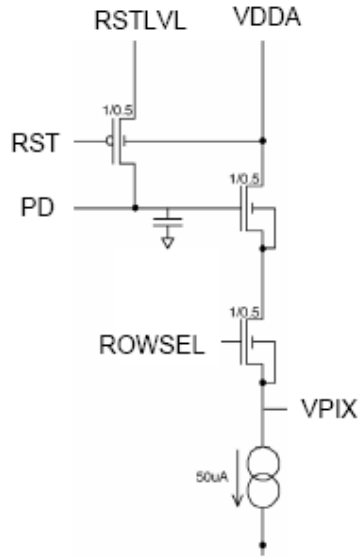
19.6.2: Cross-sectional SEM micrograph through functional active pixel imager

ISSCC 2005 / SESSION 19 / IMAGERS / 19.6

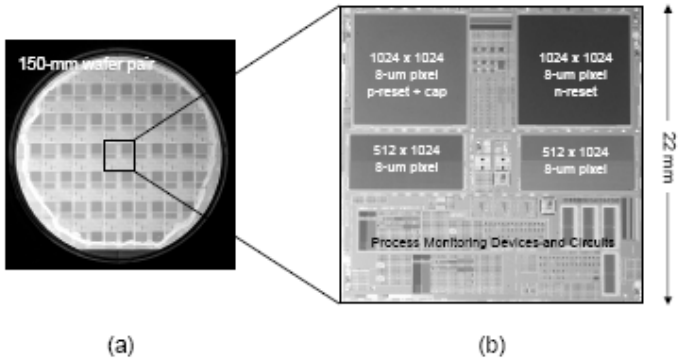
19.6 Megapixel CMOS Image Sensor Fabricated in Three-Dimensional Integrated Circuit Technology

Vyshnavi Suntharalingam, Robert Berger, James A. Burns, Chenson K. Chen, Craig L. Keast, Jeffrey M. Knecht, Renee D. Lambert, Kevin L. Newcomb, Daniel M. O'Mara, Dennis D. Rathman, David C. Shaver, Antonio M. Soares, Charles N. Stevenson, Brian M. Tyrrell, Keith Warner, Bruce D. Wheeler, Donna-Ruth W. Yost, Douglas J. Young

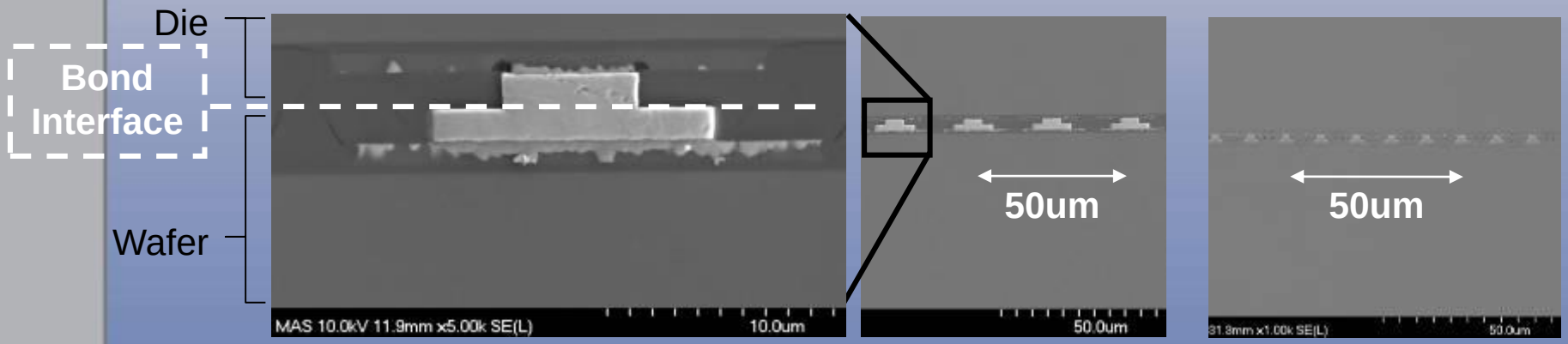
MIT, Lincoln Laboratories, Lexington, MA



19.6.3: Pixel schematic



19.6.4: (a) Completed 3D integrated wafer pair, (b) Die photomicrograph



		50um Pitch	25um Pitch	10um Pitch
	Test Part	9,950 Serial Connections	72,500 Serial Connections	1,000,000 Serial Connections
	Typical <R>	<20 mΩ (<1.5 Ω/um²)	<50 mΩ (<0.5 Ω/um²)	<50 mΩ (<0.5 Ω/um²)
Bare Die Reliability	**T cycling** (-65C - 175C)	1,000 Cycles, 18/18 PASS 10,000 Cycles, 9/9 PASS	1,000 Cycles, 5/5 PASS 10,000 Cycles, 4/4 PASS	1,000 Cycles, 10/10 PASS
	HAST (130C, 85%RH, 33psi)	96 Hours 12/12 PASS	288 Hours 6/6 PASS	

Hybridization & noise

- Going 3D brings major “goodies”
  - Optimal technology and design for each layer
  - Unprecedented functionality density

- If you leave the 2D plane you might lose other “goodies”
  - Buried photodiodes (dark current!)
  - Pinned photodiodes (CDS, low noise)
  - Low pixel interconnect capacitance (kTC noise)

Alternatives do exist but are more “*expensive*”:
- External CDS, NDR; analog or digital CDS
- Active reset, tapered reset, silencing reset

Worth remembering

- Industry technology push is directed to mainstream markets
- Ride on the wave
  - Uses the emerging [partial] technologies
  - 3D trend
    - Fine pitch
    - High yield & reliability
    - Moderate? cost (yet! # Si does not decrease!)
    - Power density?
  - Nano (2D)
    - Extreme high density of functionality
    - Has its own challenges!
      - reliability; variability; low VDD; analog