# Photon-to-Photon CMOS Imager: Opto-Electronic 3D Integration

## Image Sensors Americas 2017

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# Outline

- Key technologies for future CMOS imagers
- Bottlenecks for high speed imaging
- Our proposal
- Take home message

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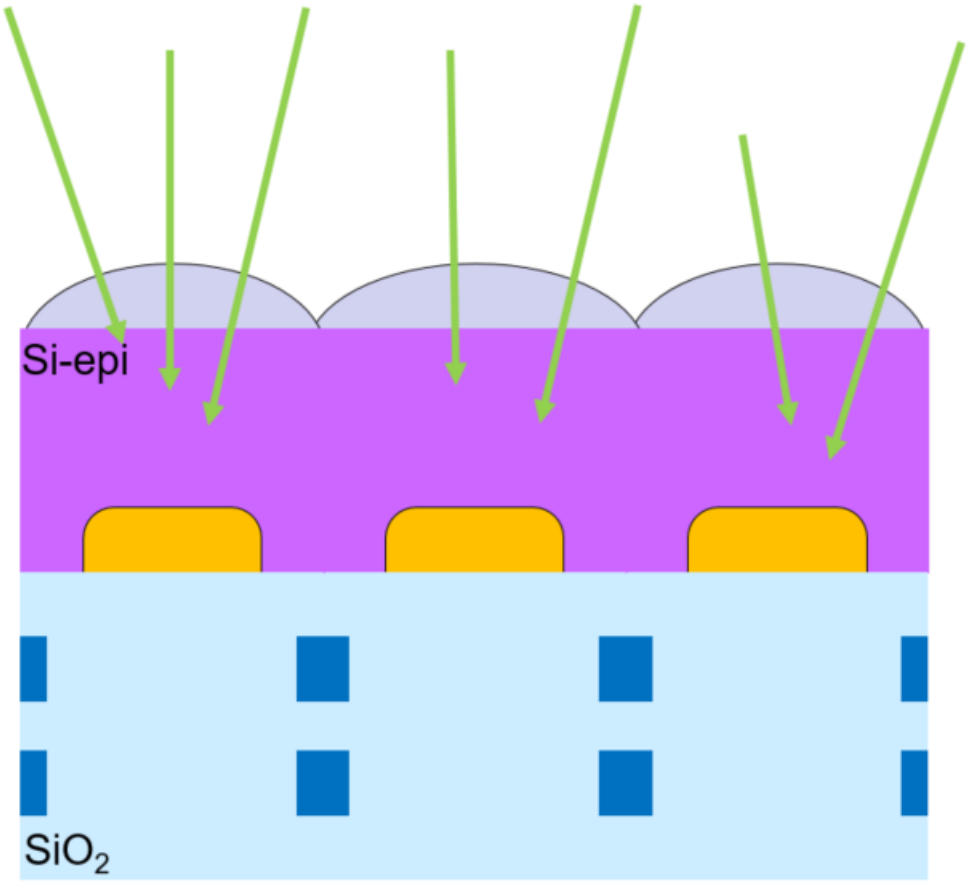
## Chapter 1

# Key technologies for future CMOS imagers

# Back-side illumination (BSI)

- Developed historically in the CCD process
- Reaches 100% fill factor
- Significantly increases quantum efficiency
- Disadvantages: complex process & cost
- First use in CMOS process OmniVision 2007
- First commercial product Sony 2009



# 3D Integration

- It is a quite old idea ( > 30 years ) !
- Akasaka Y. & Nishimura T., from Mitsubishi Electric
- “Concept and Basic Technologies for 3D-IC Structure”, IEEE IEDM, 1986, pp. 488-491

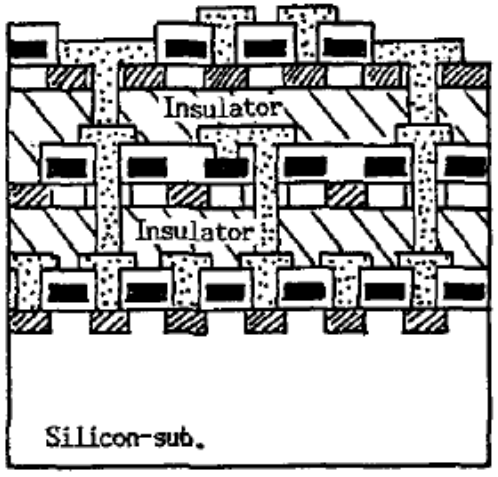



Fig.1 Schematic drawing of 3-D IC consisting of monolithic multi-layer structure.

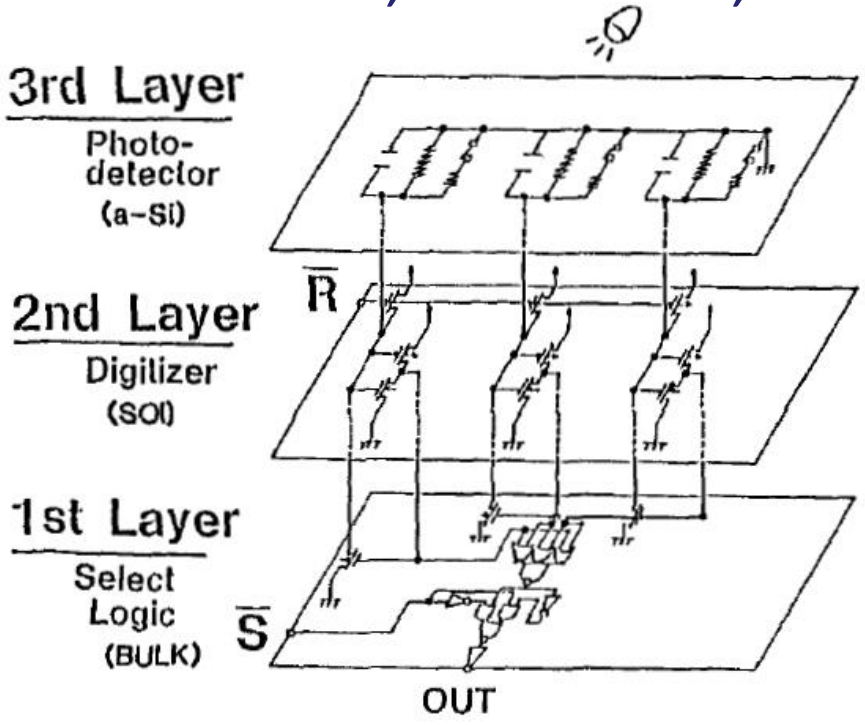



Fig.8 a-Si photo sensor and processing circuits in 3-staked layers (after Mihashi)

# TSV for image sensor

- TSV patented by W. Shockley in 1962 though not intended for 3D integration
- Sekiguchi M., et al., Toshiba

"Novel Low Cost Integration of Through Chip Interconnection and Application to CMOS Image Sensor", IEEE ECTC, 2006, pp. 1367-1374

- First time TSV (Toshiba calls it TCV) used in image sensors, but still single layer IC

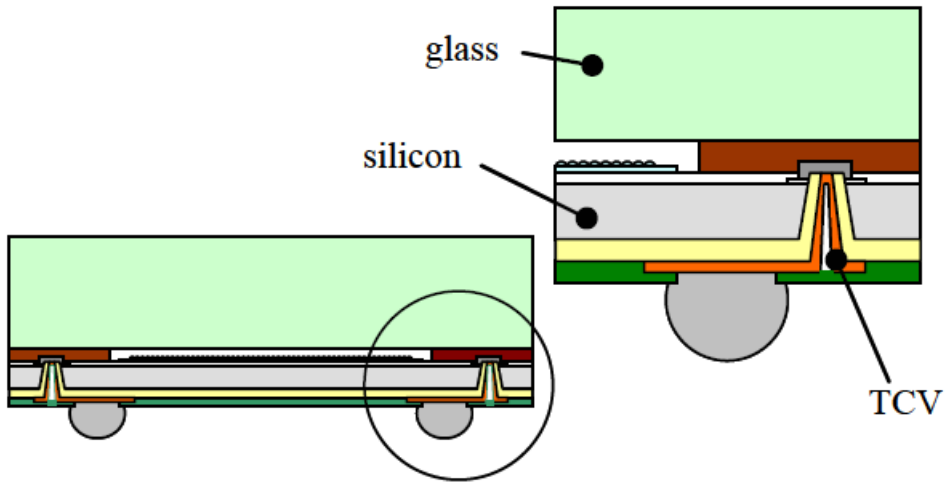



Figure 1 CMOS image sensor package with TCV

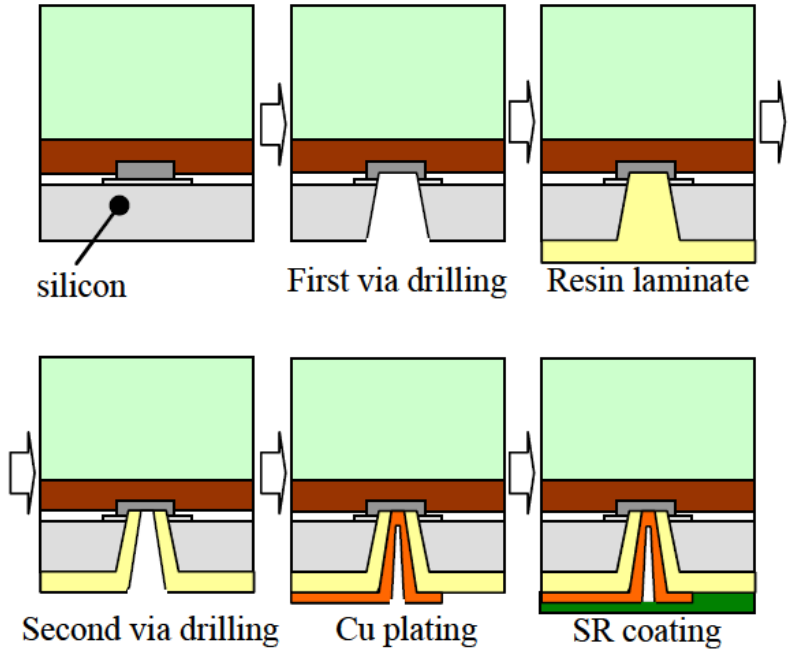
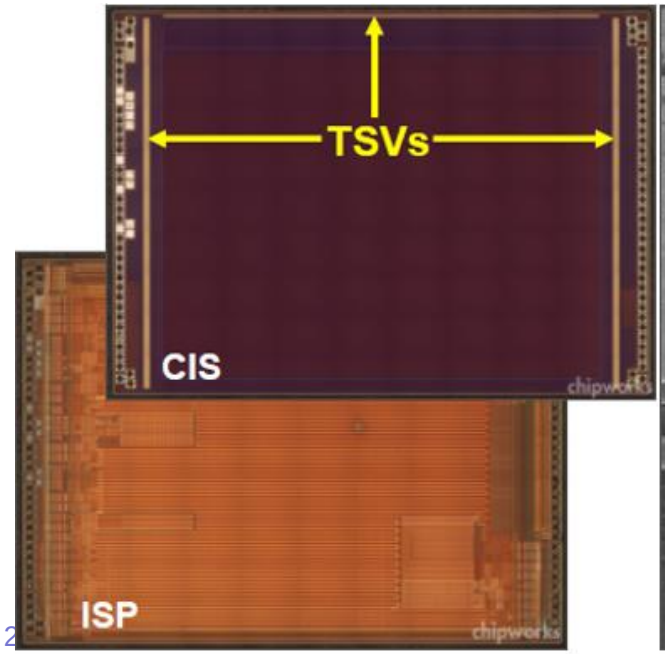
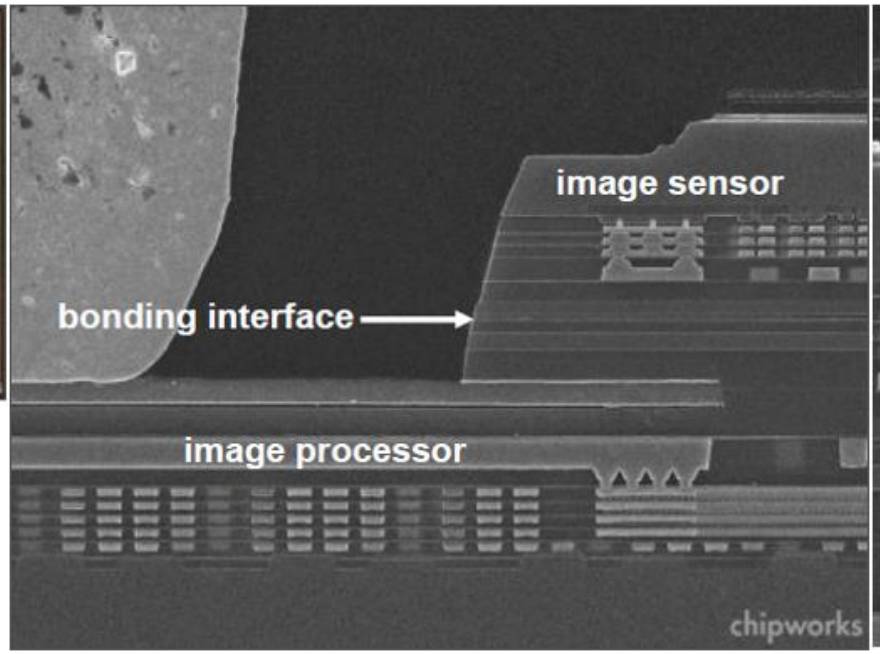


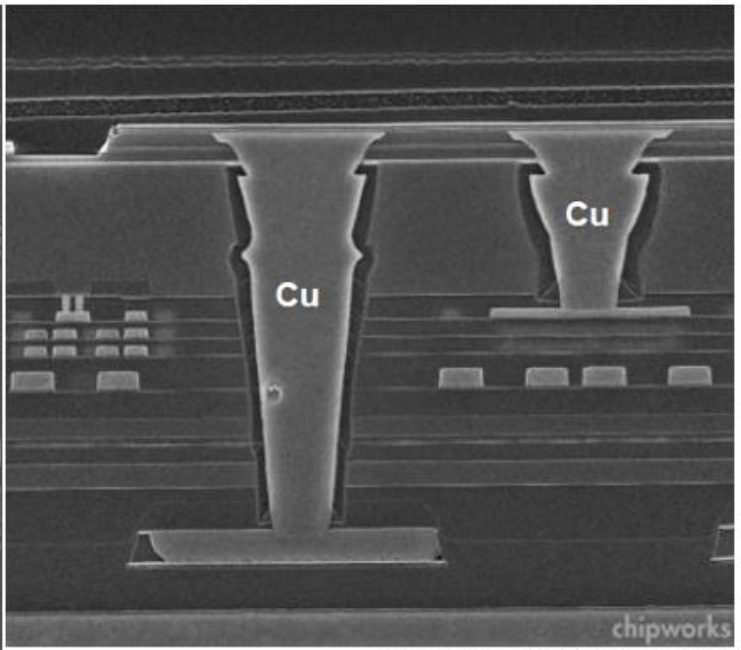

Figure 3 TCV process

# Stacked image sensor

- Milestone: Sony announced first stacked image sensors in 2012 (figures below is one of them: IMX135)
- Readout circuits still on the same layer as pixel array
- ISP locates at the bottom layer
- TSVs located at the periphery of the sensor



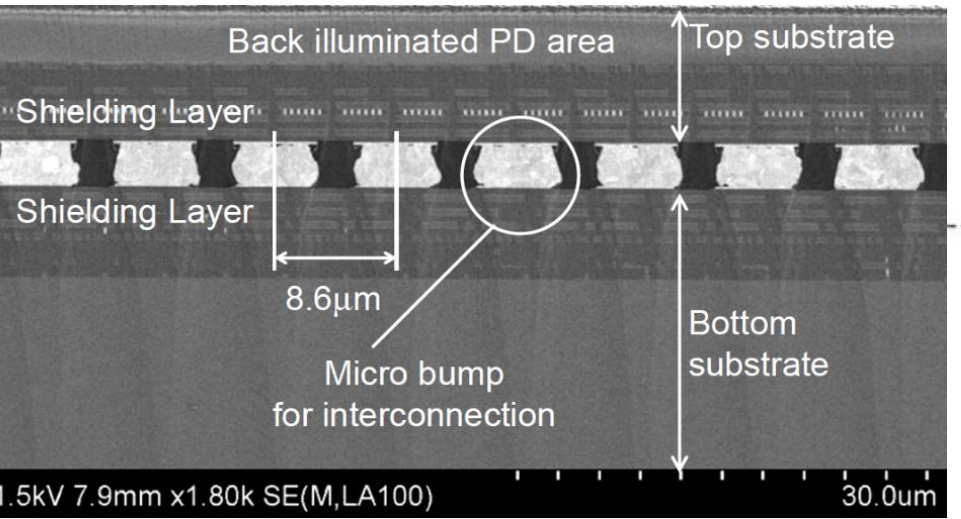



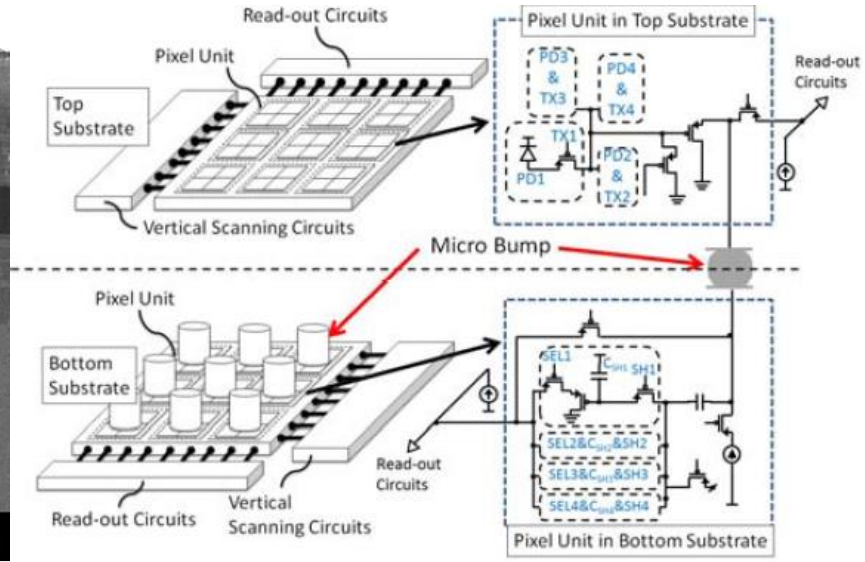



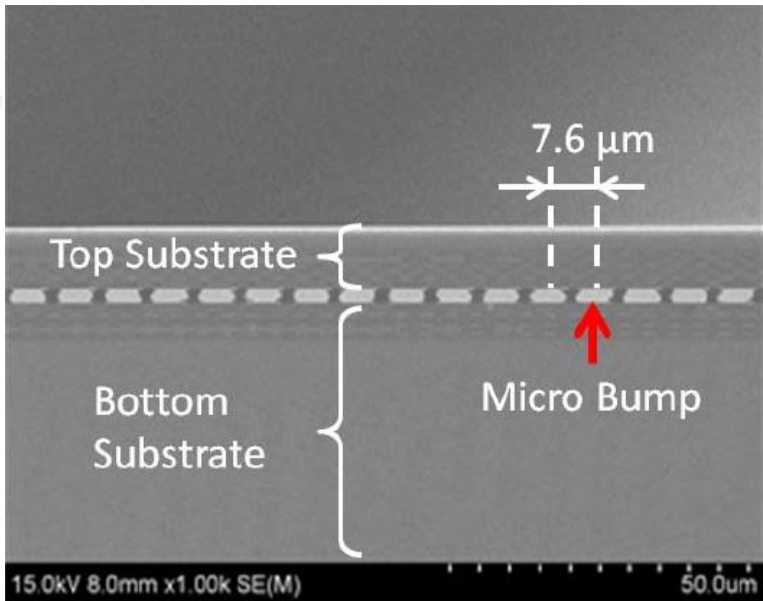

(Source: Chipworks)

# Interconnects beneath pixel array

- Olympus published stacked sensor with µ-bumps beneath pixel array at ISSCC 2013
- They later (VLSI 2015) made a much larger sensor with 4 million µ-bumps with pitch of 7.6um
- By doing so, they can achieve excellent PLS for 16Mpixel global-shutter mode and 10,000 fps for 2Mpixel rolling-shutter mode



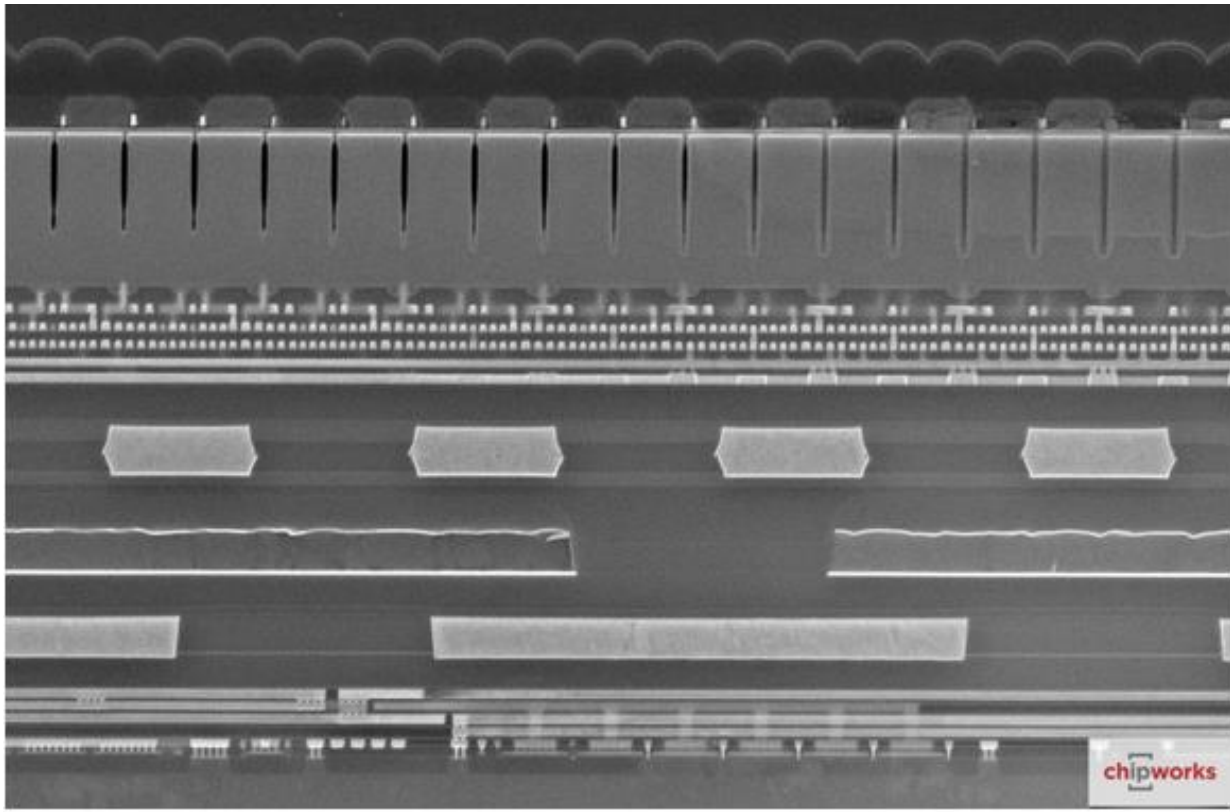



# Direct Cu-Cu bonding

- Several solutions exist such as:
  - Surface-activated bonding
  - Cu nano-rod bonding
  - Solid-Liquid Inter-Diffusion bonding (SLID)
  - Direct Bond Interconnect (DBI®)
  - etc.
- DBI® is developed by Ziptronix (acquired by Tessera, now Xperi)
  - Direct oxide bonding at room temperature

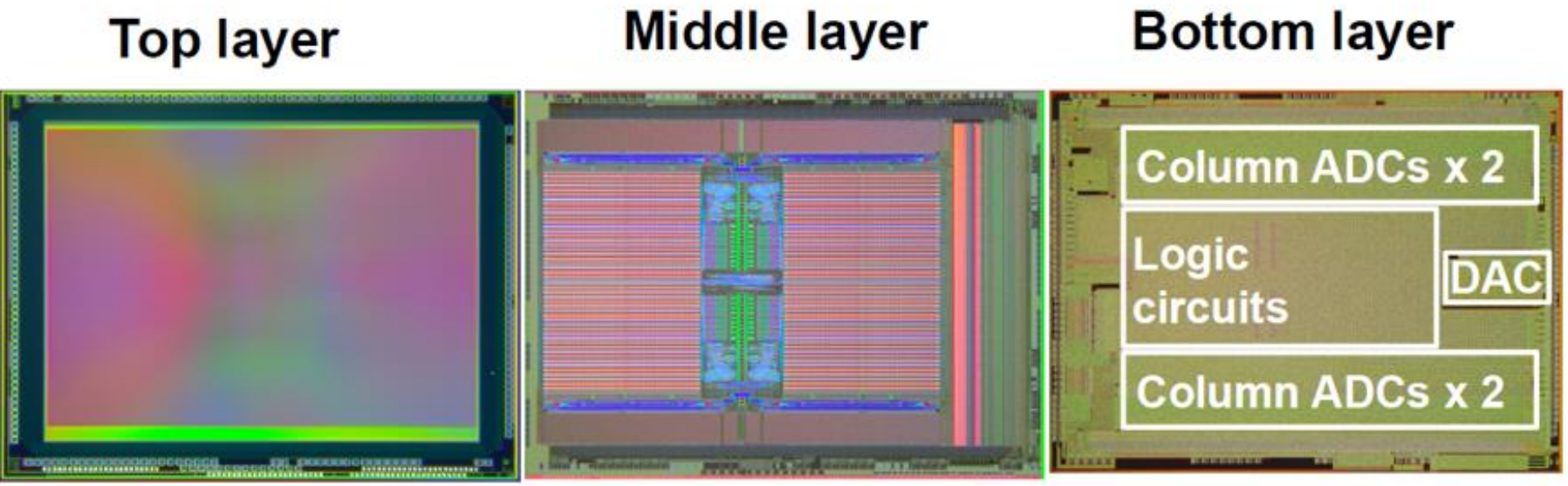
- Cu-Cu bonding with low temperature anneal (150-300°C)
- Good scalability (pitch < 2µm)

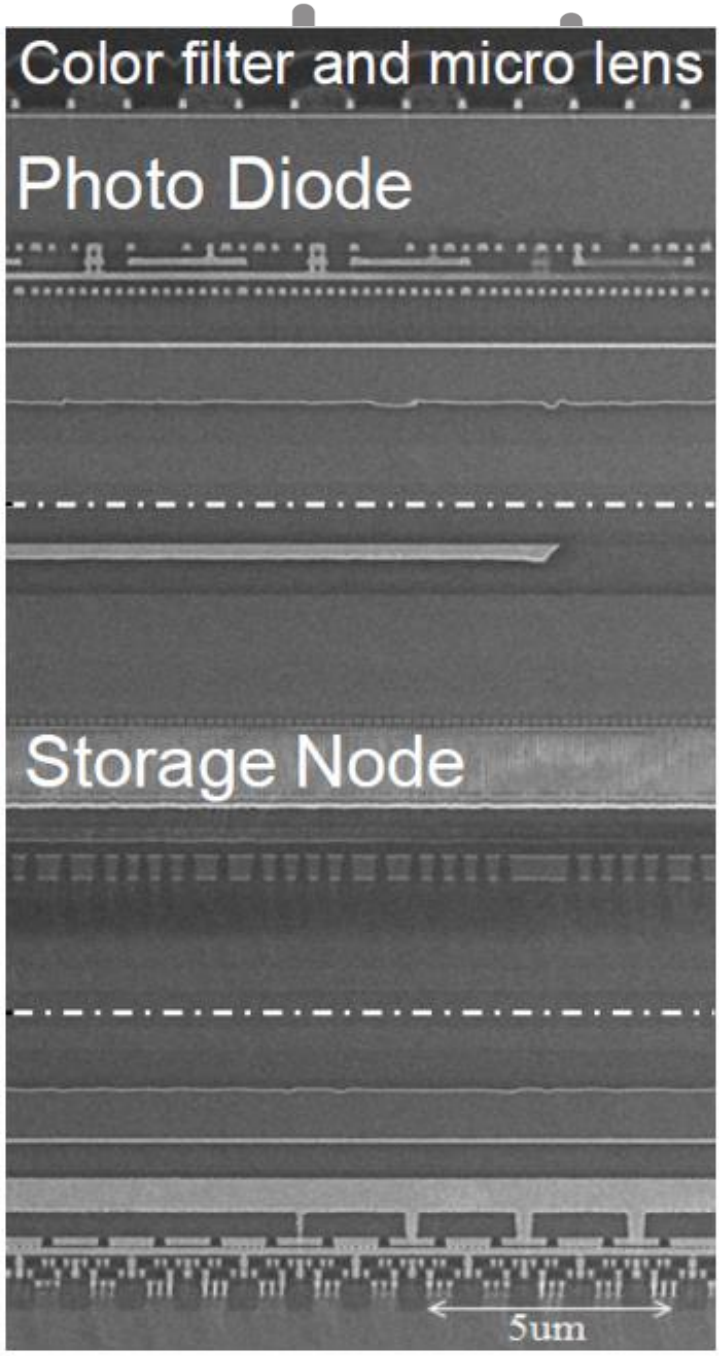



(Sony IMX260, Source: Chipworks)

# 3-layer stacked imager

- State-of-the-Art: published in ISSCC 2017
- Sony product: IMX400
- TSVs are used to connect Pixel array with Logic & Logic with DRAM




(Source: ISSCC 2017)

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## Chapter 2

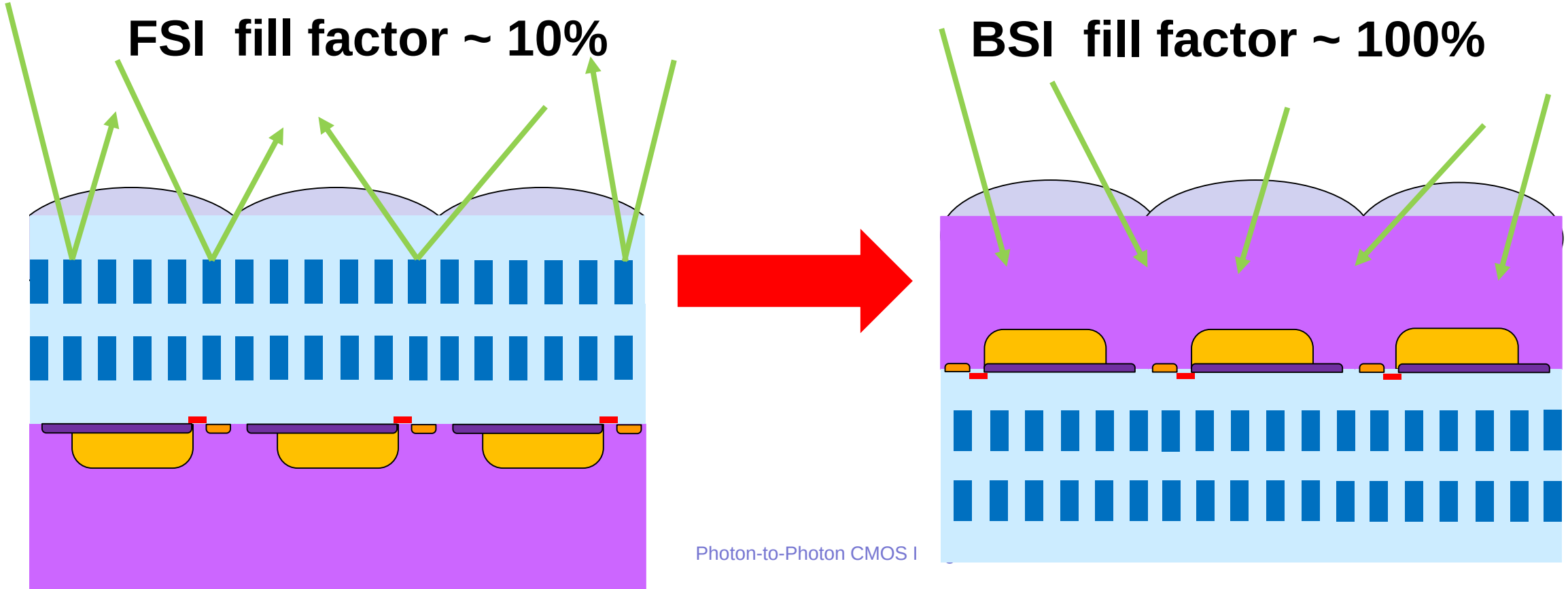
# Bottlenecks for high speed imaging

# Reflection on interconnect metal

In order to reach high speed

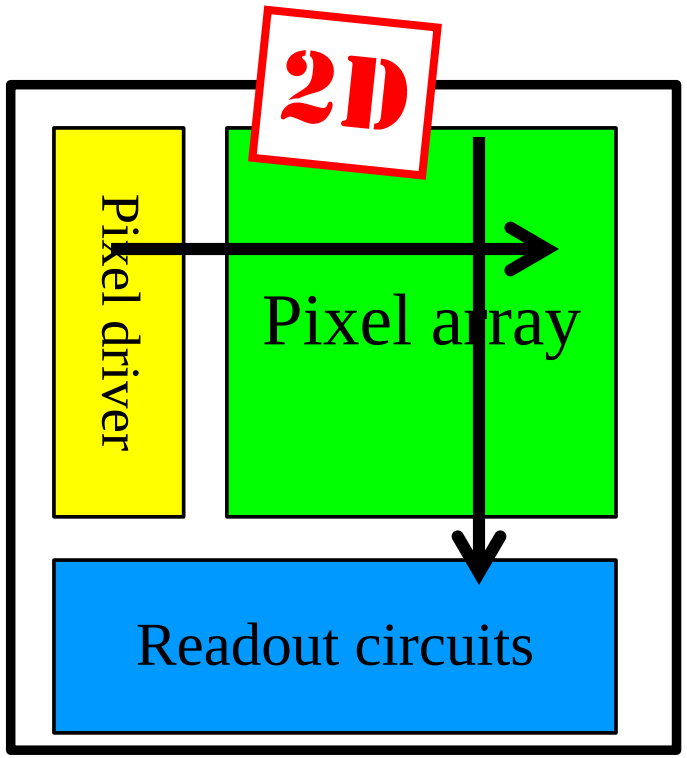
⇒readout multiple rows of pixels simultaneously

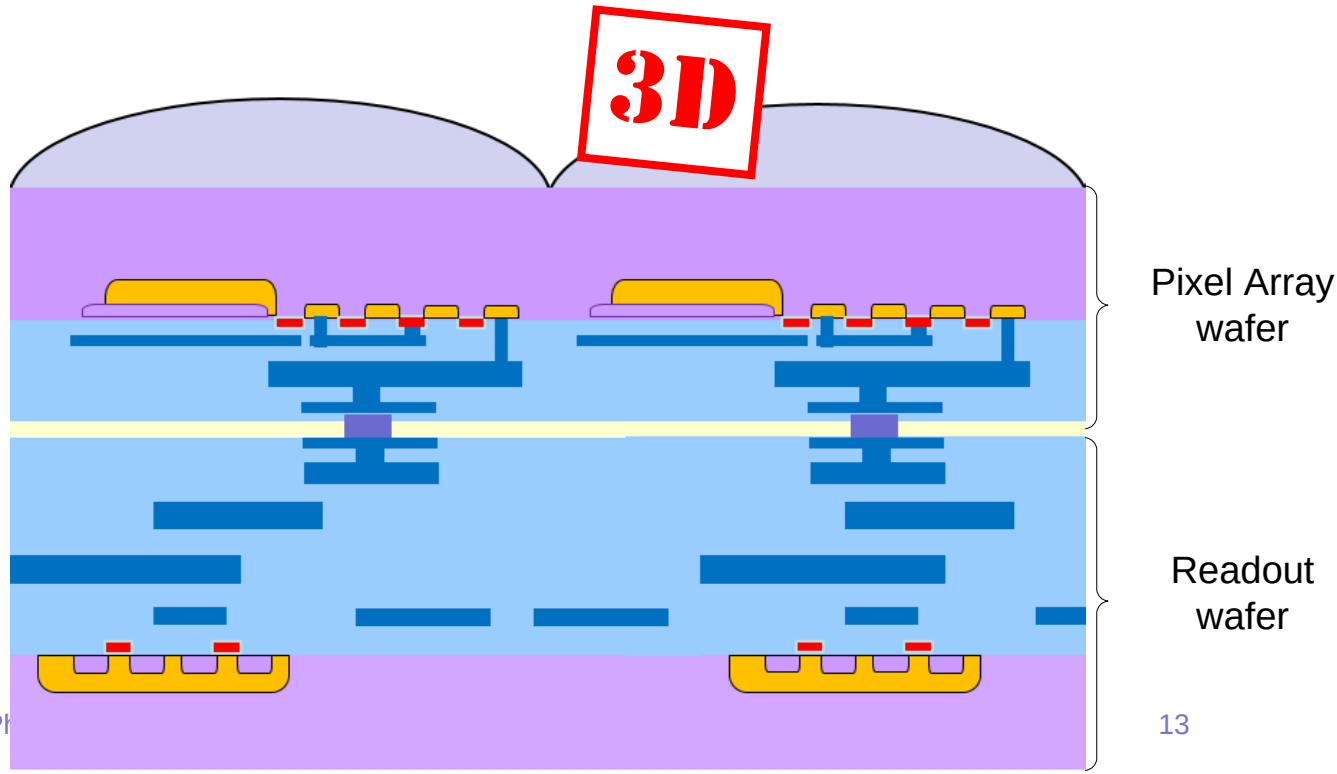
⇒many metal wires cover the front side of the pixel



# *Long* metal wires

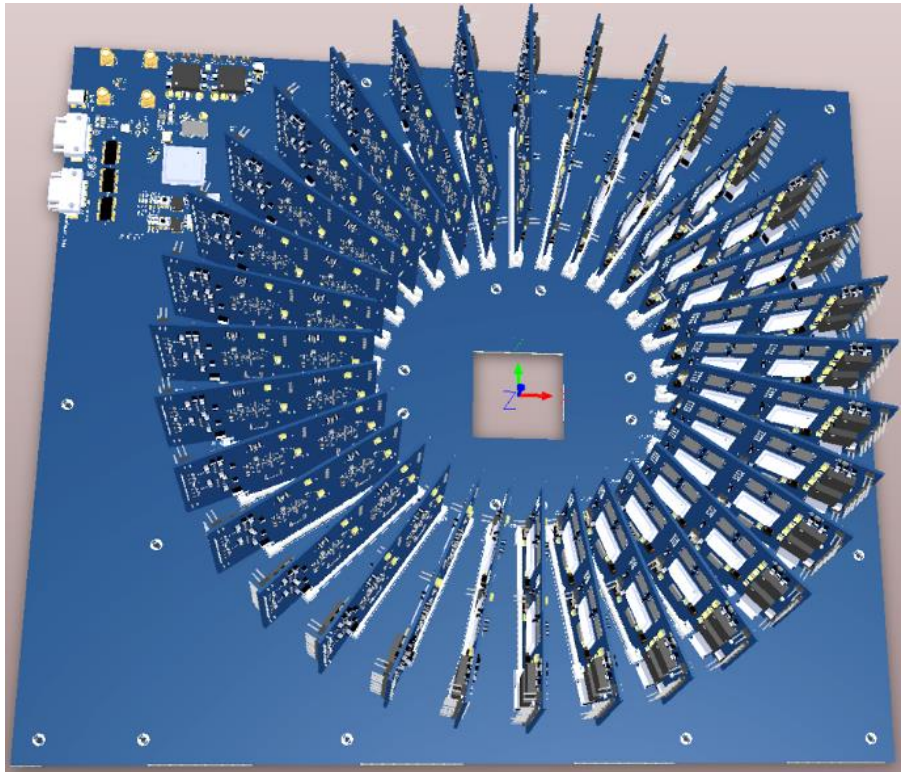
- In conventional 2D imagers, row and column wires run over the whole (or at least half) the pixel array
- The longer the column wires, the slower the readout speed
- The longer the row wires, the slower the access times



# High number of I/O

- High number of I/O are required to handle the high date rate
- Complex system, high power consumption
- Signal integrity degrades significantly at high speed on the board which further makes the design more difficult



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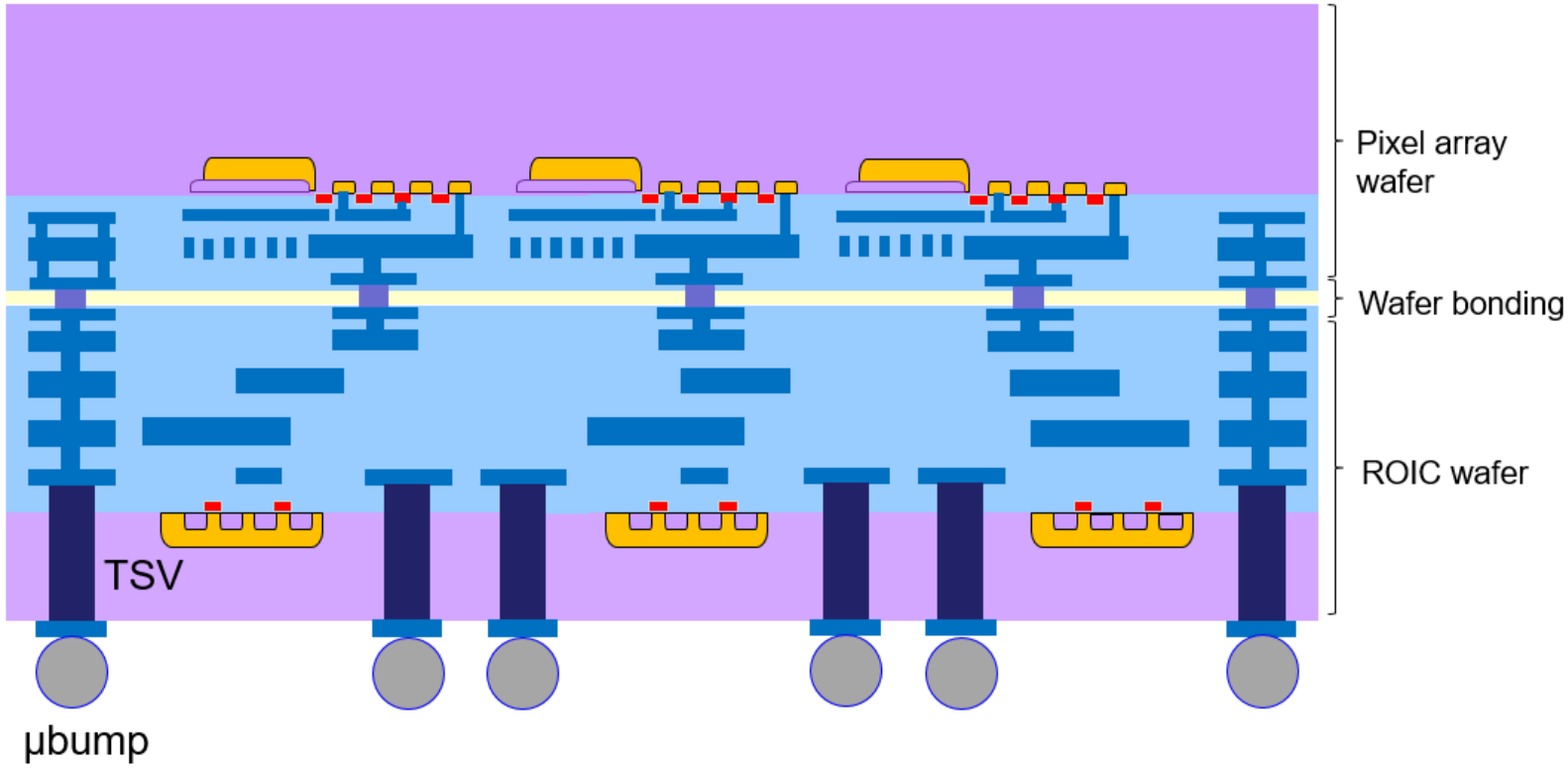
## Chapter 3

# Our proposal

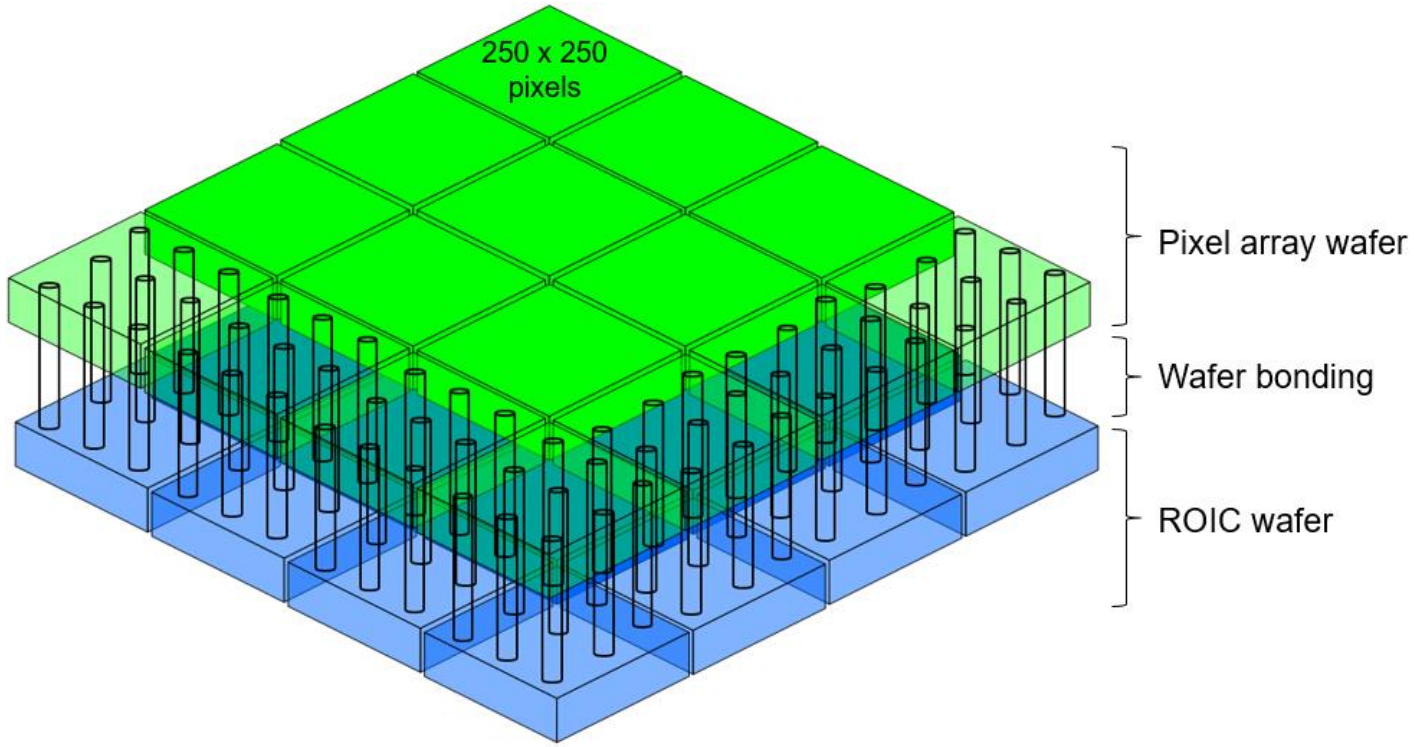
# Prior art - BSI & Wafer stacking

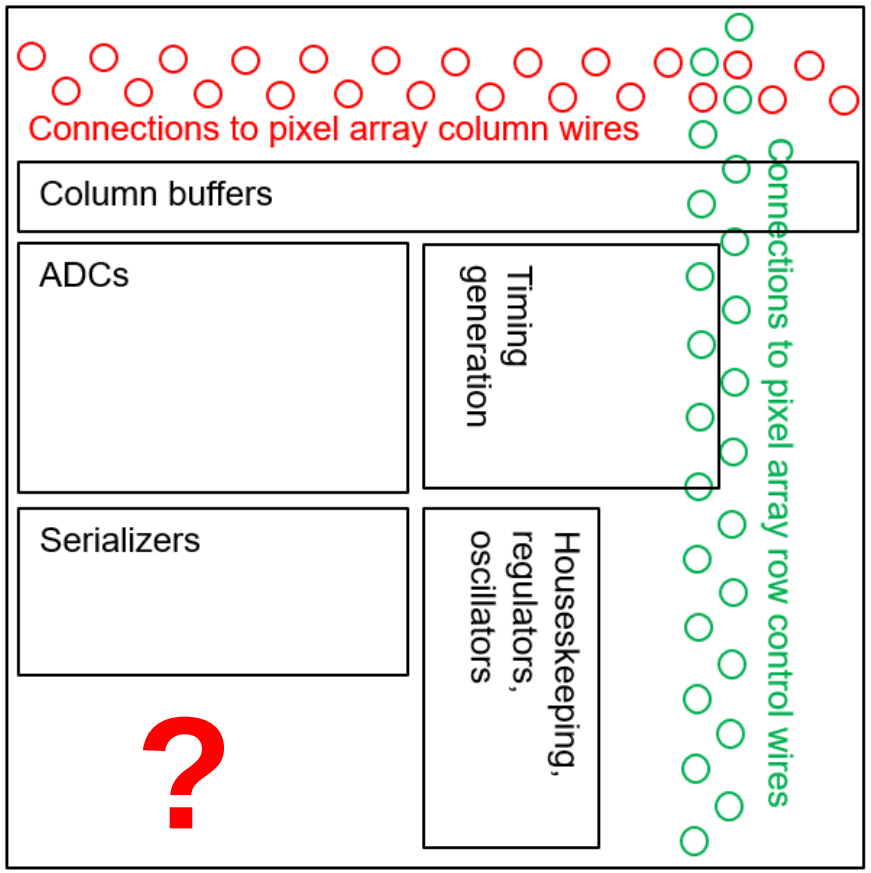
- BSI for the imager layer: solves metal reflection fill factor limitation
- Just doing wafer stacking does not solve the long metal wires issue, further improvement is needed



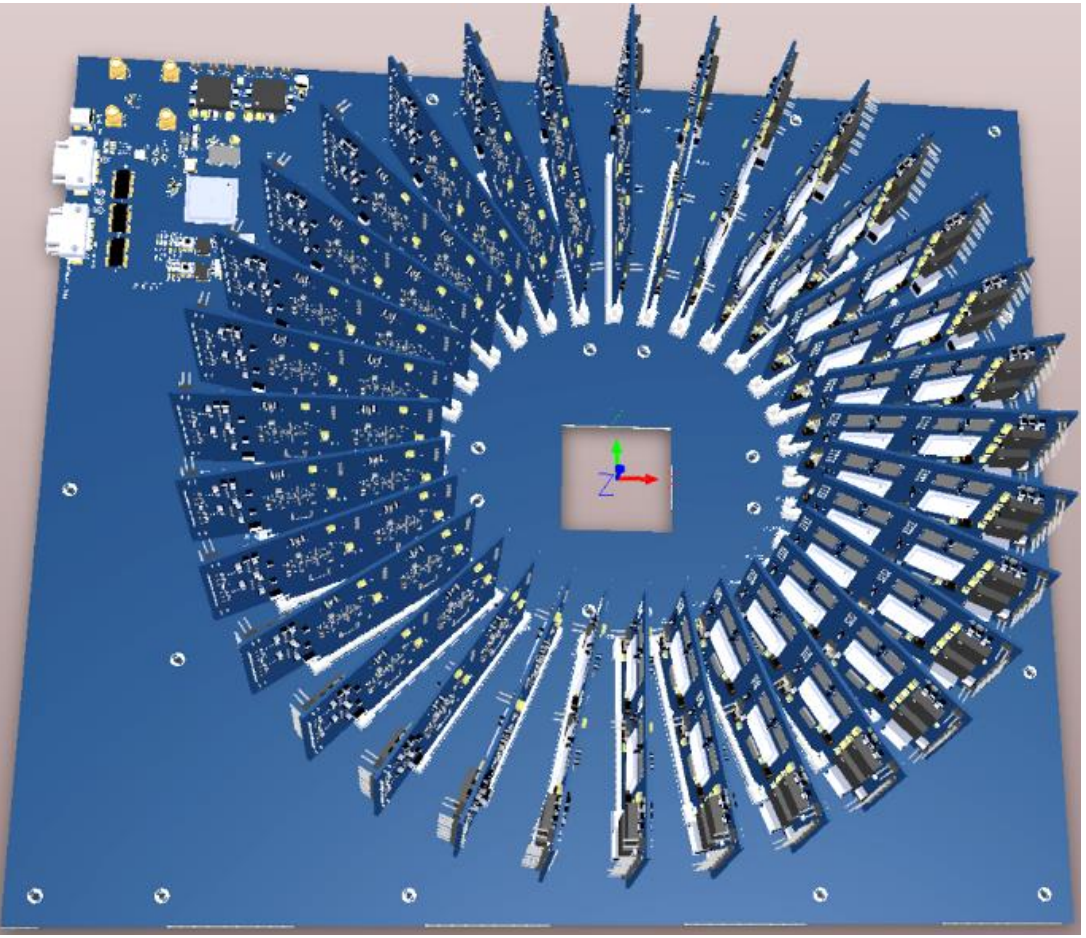
# Proposal a) divide in “tiles”

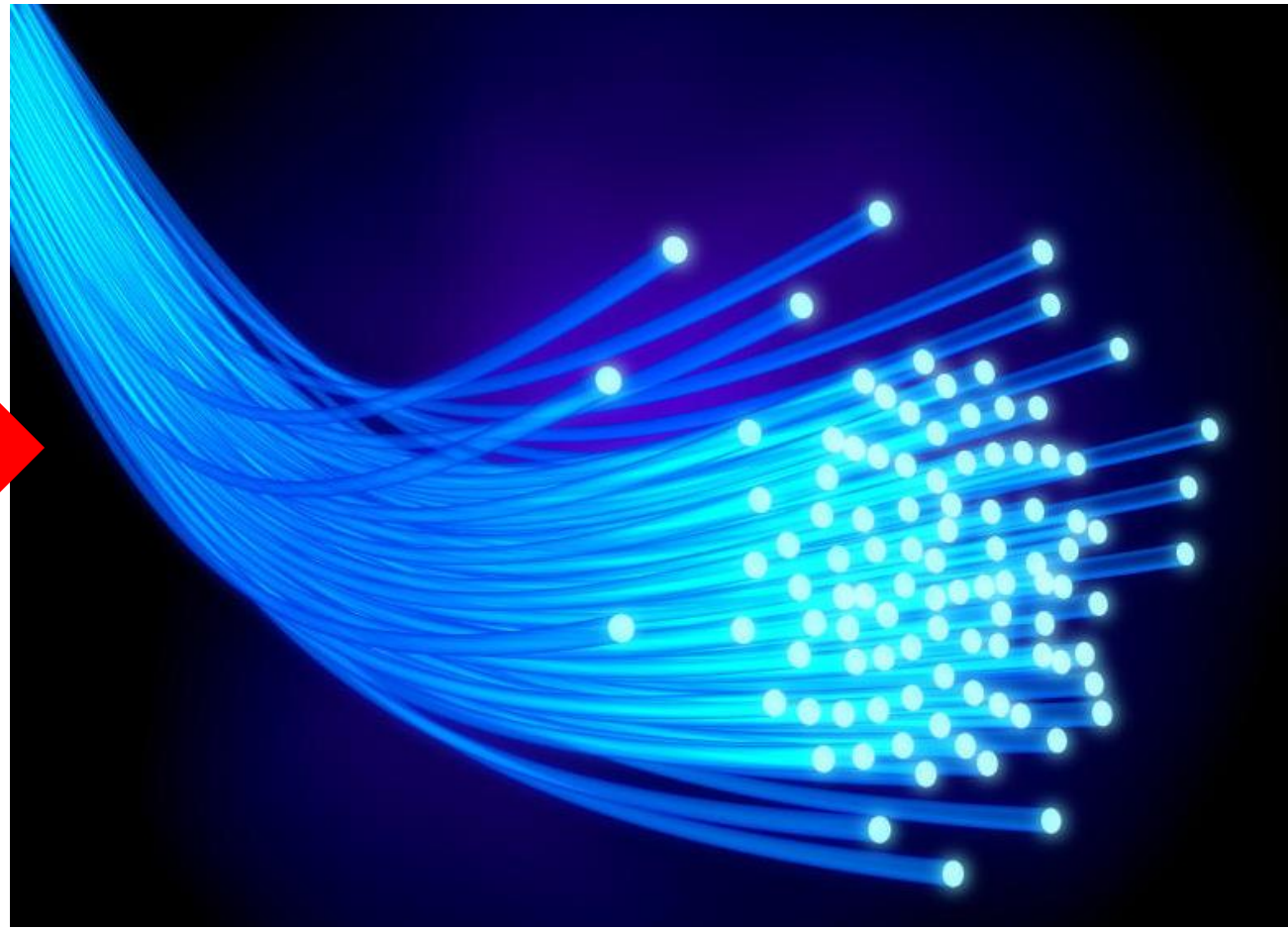
- The entire array should be split into sub-arrays (or “tiles”) so that column/row wires are segmented and short
- Beneath each pixel tile (e.g. 250x250 pixels), there is readout IC (ROIC) tile
- Each ROIC tile is self-contained



# High number of I/O? An optical link layer (-tile)





# Rationale

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**Problems with Electrical Link:**

a. Signal attenuation at high speed
b. Crosstalk between channels
c. Limited link distance
d. Power consumption (drivers, pre-emphasis, equalization, overhead…)
e. Bandwidth of electrical wires

**Advantages of Optical Link:**

a. High data rate density
b. Much less crosstalk
c. Much longer distance in optical fibers
d. Potentially lower on-chip power dissipation (laser is outside!)
e. Wavelength Division Multiplexing (WDM) further increases the bandwidth density

# Add photonic IC

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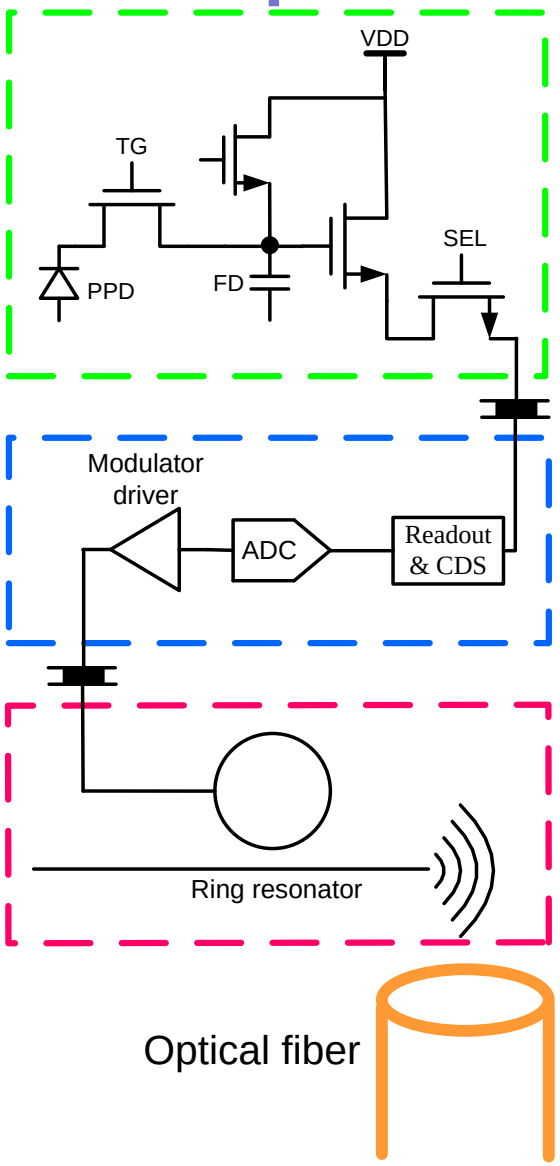
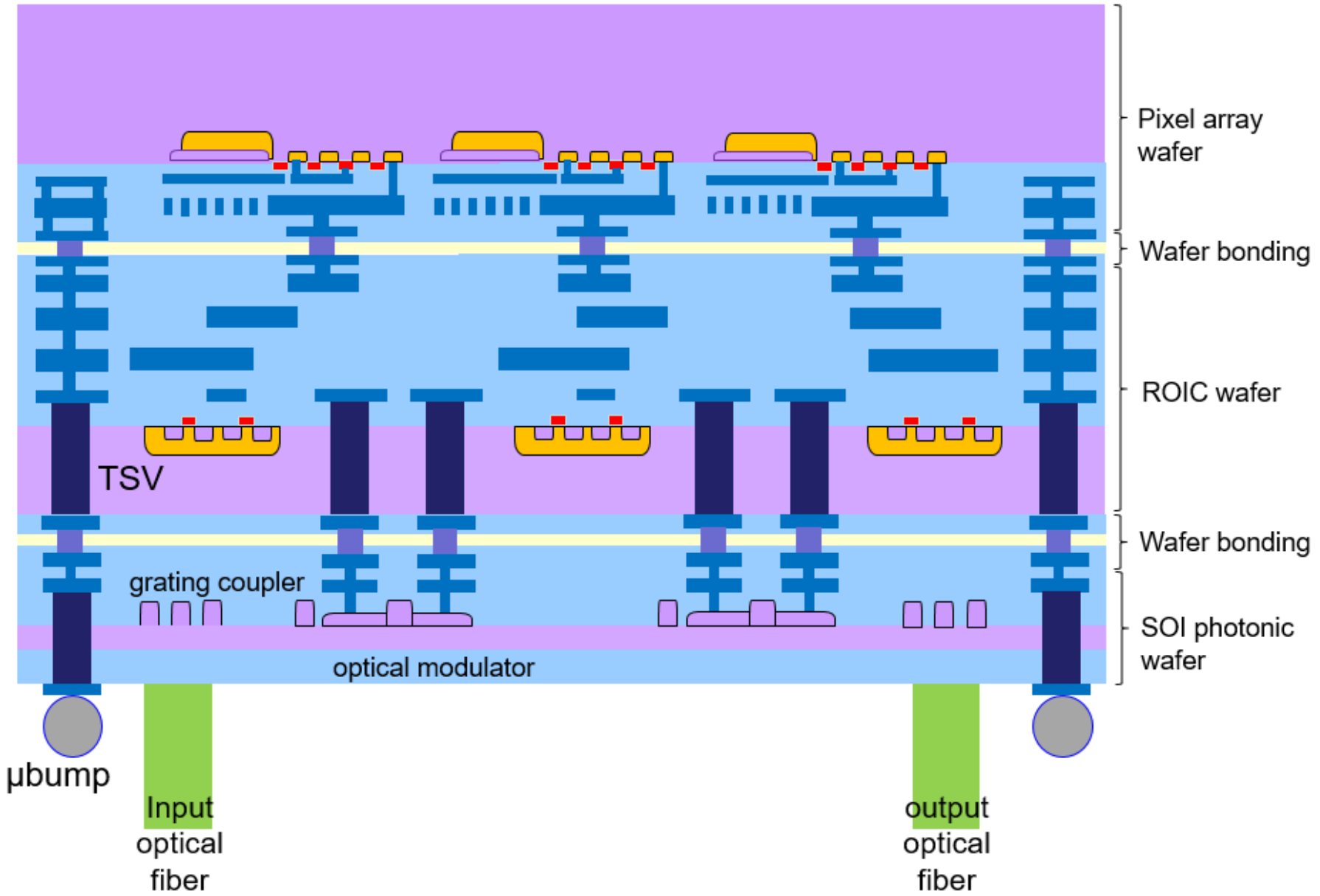
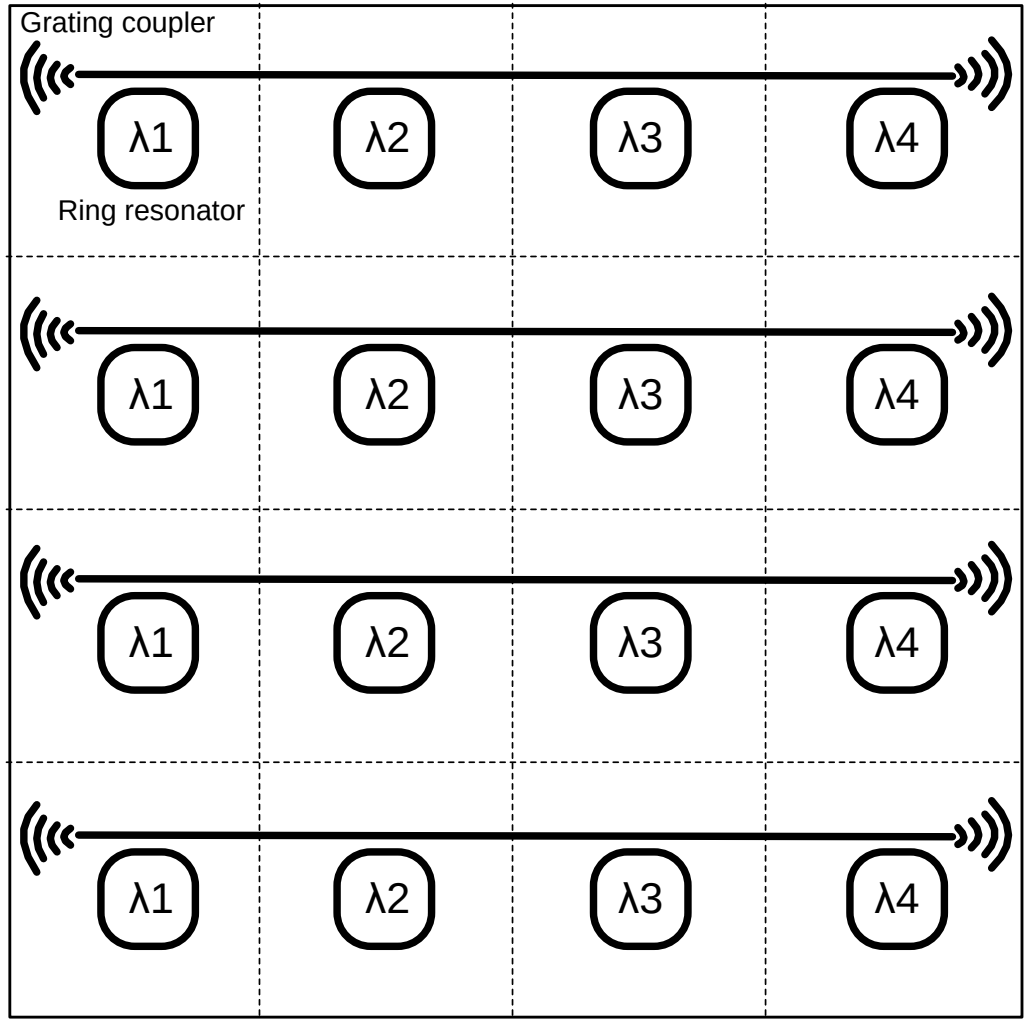
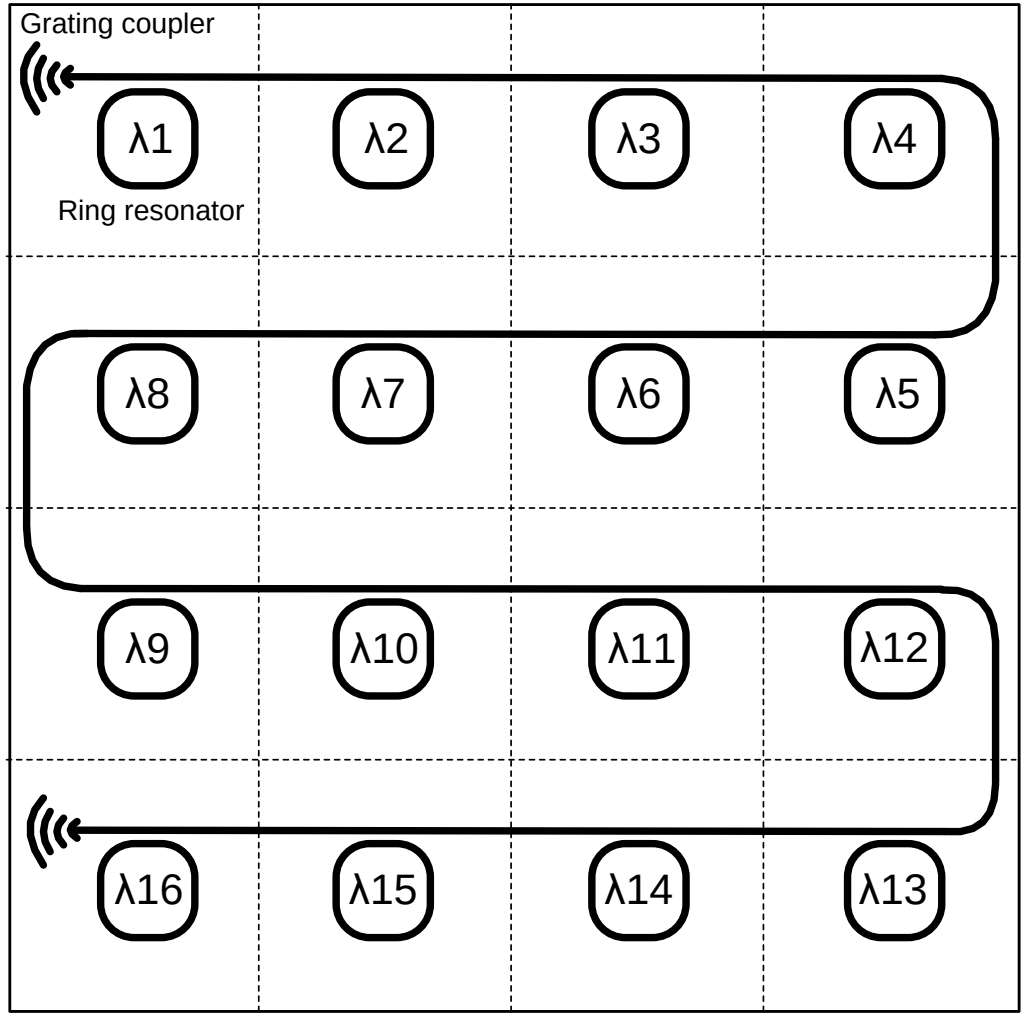


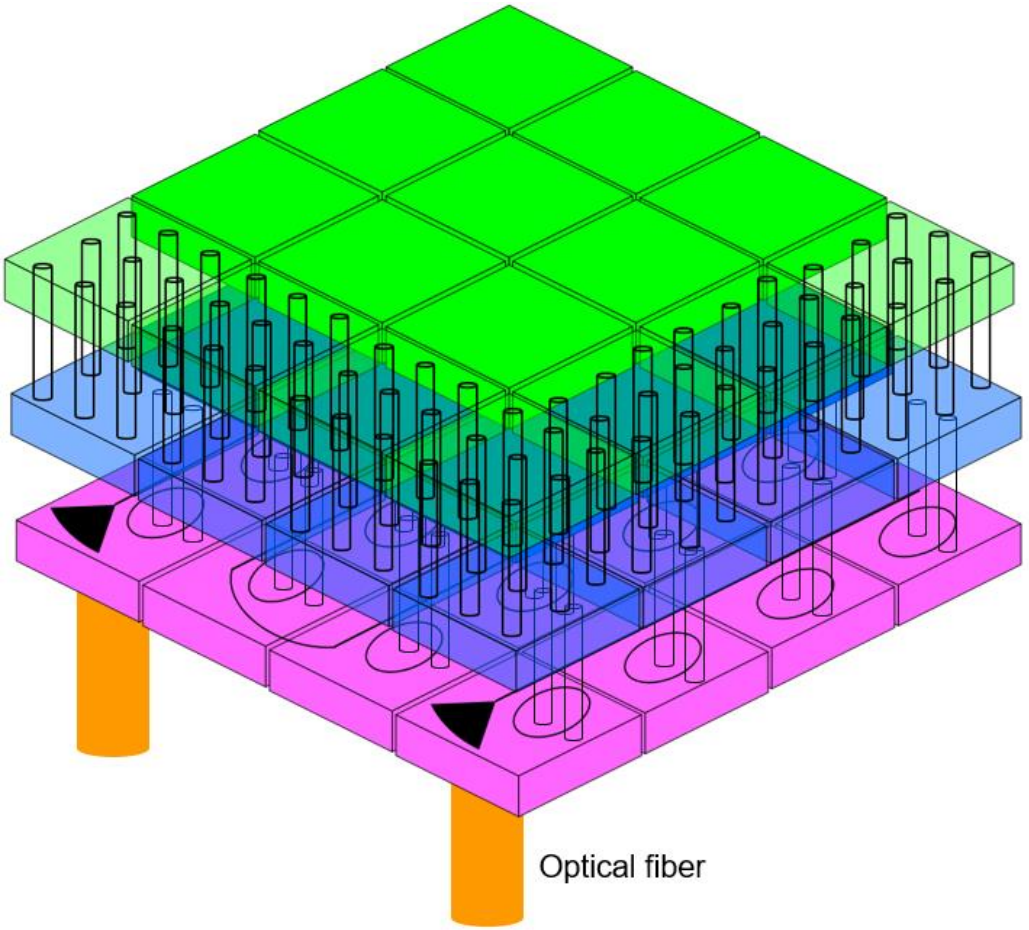



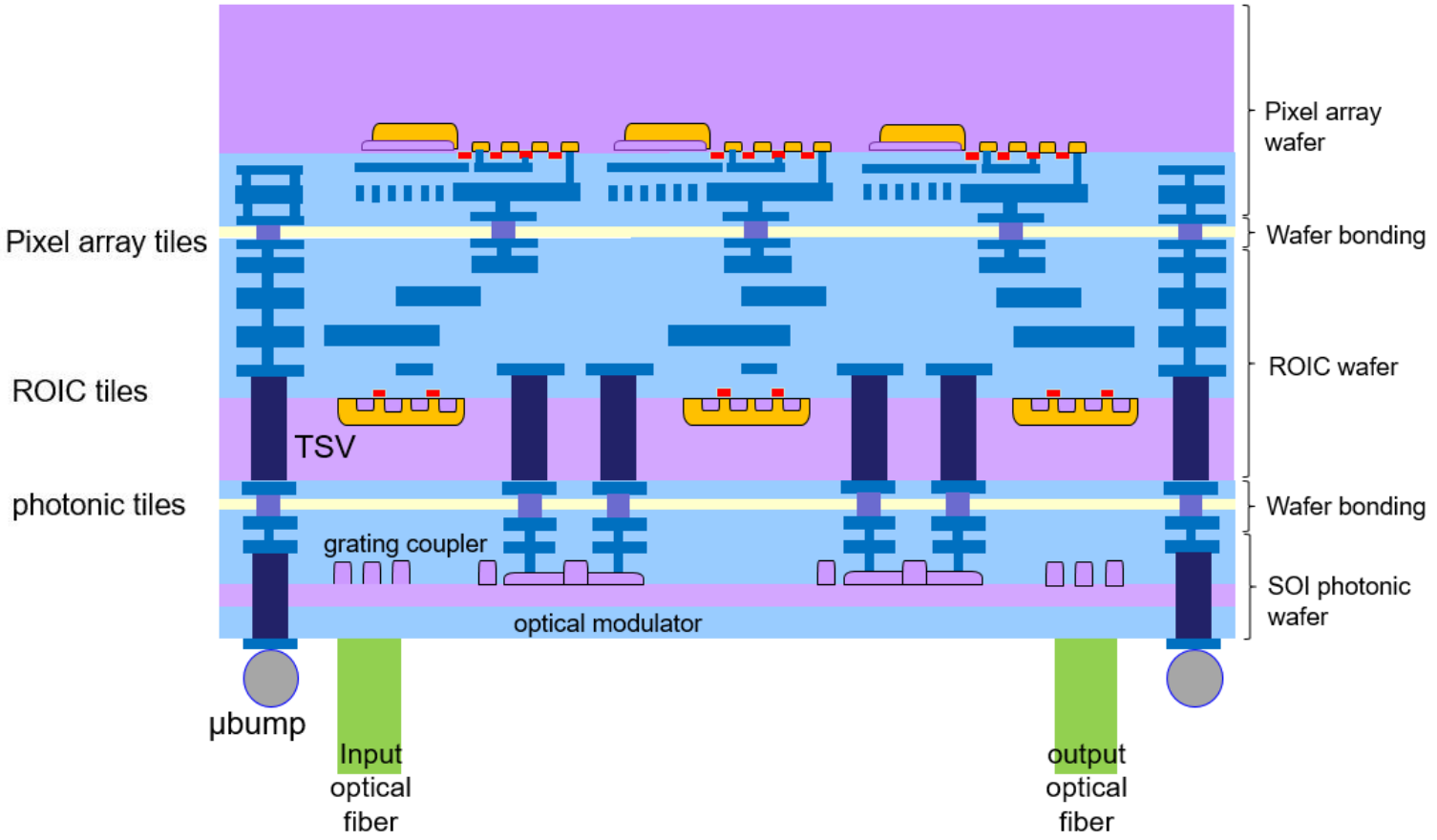
# Wavelength division multiplexing (WDM)



# Final solution



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## Chapter 4

# Take home message

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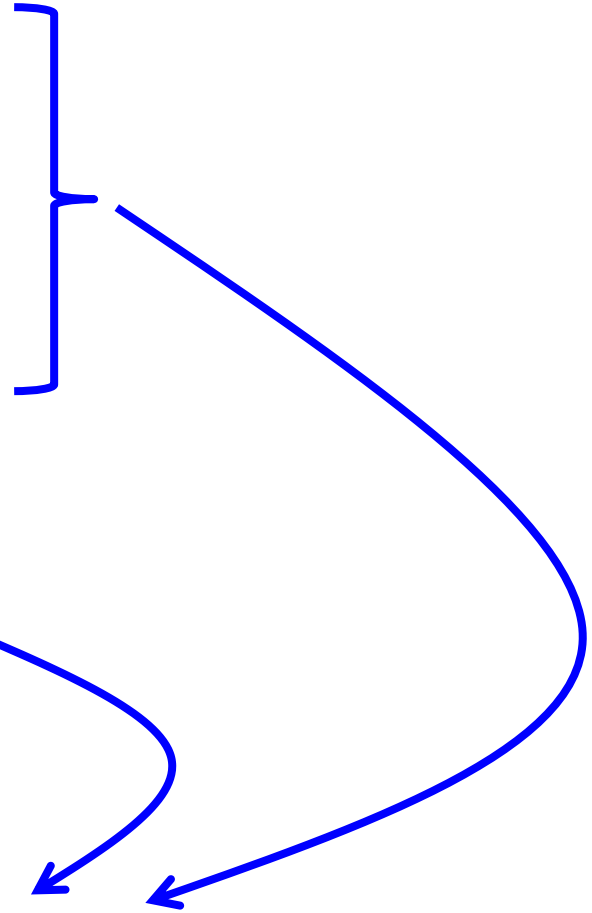
- Key technologies for future CMOS imagers
  - BSI
  - 3D integration
  - Photonic IC
- Bottlenecks for high speed imaging
  - Metal reflection
  - Long metal wires
  - High I/O counts
- Solution for high speed imaging
  - Add silicon photonic IC as third layer
  - WDM to increase date rate and reduce I/O counts



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