Multiple shutter mode radiation hard IR detector ROIC

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A generic radiation hard IR detector readout IC (ROIC) for cryogenic temperature operation with an array size of 320 (H) x 1080 (V) that is capable to interface with long wave (>10um) to short wave (<2um) IR detector focal plane arrays is implemented. It operates at over 20 fps in four shutter modes: integrate while read (IWR), integrate then read (ITR), rolling shutter (RS) and non-destructive readout (NDR) or Fowler sampling. The 20 µm pixel contains a capacitive trans-impedance amplifier (CTIA) with 3 in-pixel sample and hold (S&H) capacitors. Programmable integration capacitors provide dual gain full well of 10ke- and 50ke- for a voltage swing of 2 V. The read noise is < 35e-, measured at room temperature. The reset and integrated signal values of the CTIA are converted to differential signals in the column-based correlated double sampling (CDS) stage. Devices are manufactured in XFAB-XS018 technology.

Introduction

An infrared imager typically consists of a detector diode array (realized in HgCdTe (MCT), GaAs etc) pixel to pixel bonded onto the ROIC (realized in silicon) through Indium bumps [1]. The detector diodes convert the incident IR radiation to proportional quantity of electrons. For high-sensitivity at longer wavelengths, detectors are realized with narrow bandgap semiconductor materials. The narrow bandgap of the detectors results in high dark current, unless they are cooled down to cryogenic temperatures. In addition to above requirements, certain applications might require the device to be operated at extreme radiation conditions.

The above-mentioned detector characteristics requires the design of readout electronics that is compatible with cryogenic operation and is radiation hard. The cryogenic operation also implies that the chip operates with very low power consumption. In most cases this is compatible with the requirement for very long integration times [2].

The narrow bandgap of the detector requires very accurate and stable biasing. The transients on the detector bias voltage results in image artifacts which are difficult to calibrate. In that respect CTIA based pixels are superior over other topologies: the CTIA's feedback maintains an accurate and stable bias voltage on the detector [3][4], with additional measures to minimize the transients. The architecture of our CTIA enables the readout of both 'P over N' or 'N over P' detector diode types.

The yield of the non-Silicon detectors is much lower than the CMOS ROIC yield. The defect detectors could be excess dark current generation center or worse a short between their bias terminals. The defect detectors can also bloom the neighboring detectors. An in-pixel programmable switch between the bump pad and virtual ground of the CTIA allows to disconnect the defect detectors from the ROIC.

Many integration modes are available: IWR, ITR and RS. Non-destructive readout is possible as well and is often the choice in deep space astronomy where integration times are extremely long and very low read noise must be reached.

The ROIC is implemented with the specification shown in Table 1.

Array size	4x320 (H) X 1080 (V)
Pixel pitch	20 µm
Integration modes	Integrate While Read (IWR) Integrate Then Read (ITR) Rolling shutter (RS) Non-Destructive Readout (NDR)
Radiation hardness	TID, SEU, SEL
Programmable Integration capacitance	8 fF 40 fF
Diode compatibility	P over N N over P
Pixel readout rate	20 MHz
Operating temperature	40 K - 80 K
Technology	0.18µm XFAB

Table 1: Specifications

In the following sections pixel topology, pixel noise analysis, layout for radiation hardness is discussed. Test pixels for measurements without the detectors being bonded and some measurement results are followed.

Pixel topology

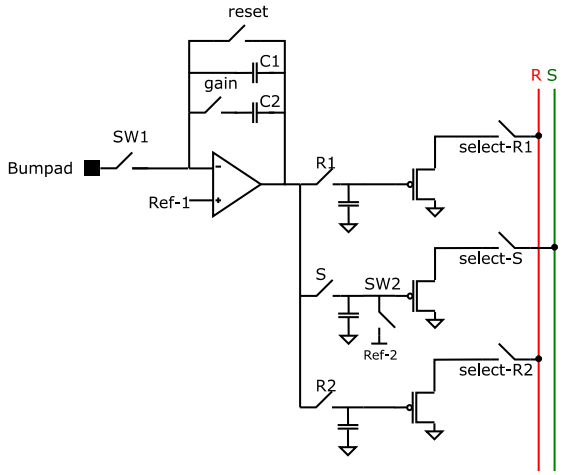


Figure 1: Schematic of pixel

Figure 1 is the schematic representation of the pixel. The detector is bonded on the bump pad and connects to the virtual ground of the amplifier through programmable switch ‘SW1’. Switch SW1 is programmed to disconnect a faulty detector from ROIC. The 8fF integration capacitor ‘C1’ is designed to contain 10Ke-. An additional 32fF capacitor ‘C2’ can be connected by programming switch ‘gain’. The reset voltage of the amplifier can be sampled on capacitors connected through switch ‘R1’ and ‘R2’. The integrated amplifier output signal can be sampled on capacitor connected through switch ‘S’. The signal sampling capacitor is discharged before sampling via switch ‘SW2’.

The sampled voltages on the capacitor are buffered onto the columns through PMOS source followers.

All the switches are complementary in nature to overcome the reduced signal handling range of NMOS/PMOS only switches at cryogenic temperatures.

Pixel operation

The operation of the pixel in IWR mode is shown through the timing diagram in Figure 2. IWR mode requires the use of the pixel’s all three S&H capacitors. ITR and RS operation can be achieved with only 2 S&H capacitors.

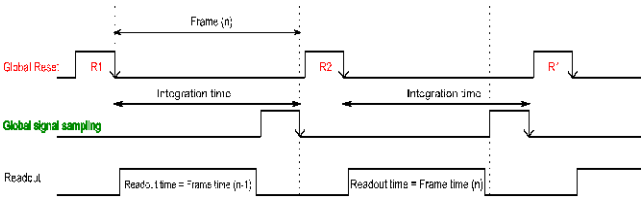


Figure 2: Timing diagram of IWR mode

The chip is globally reset and the reset level is sampled on the capacitor connected through the ‘R1’ switch. During the integration time, the previously sampled integrated signal is readout, shown as ‘Frame time(n-1)’. After the frame readout, the signal sampling capacitor is pre-charged and the integrated voltage at the output of the amplifier is sampled. The pixel is reset again and the new reset level is sampled on the capacitor connected through switch ‘R2’. The readout of the sampled frame is done while the pixels are in integration.

Similarly, the ITR and RS mode follows with usage of capacitor ‘R1’ and ‘S’.

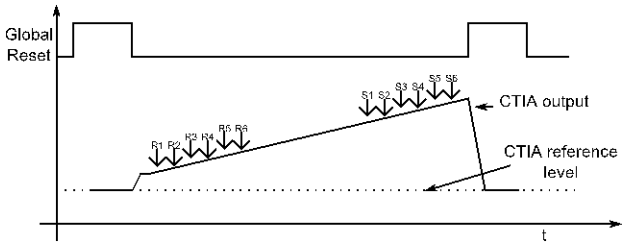


Figure 3: Non-destructive readout (NDR)

The timing of Non-destructive readout is shown in Figure 3. The sequence starts with a pixel reset. The CTIA output is read out consecutively with or without using the S&H stages. The minimum time difference between two readouts is a frame time if all the pixel rows are read. 'n' reset frames and 'n' signal frames are readout during one integration time and subsequent signal processing is done off-chip. In this mode, zero, one or all the three S&H capacitors can be connected in parallel as load to the CTIA. This reduces the bandwidth of the amplifier and impacts the total integrated noise at its output.

Noise analysis

The overall noise of the pixel shown in Figure 1 has multiple contributions, as: dark current shot noise of the detector, resistive and capacitive coupling of detector bias noise, and the noise due to ROIC. The CTIA operation noise can be separated in 2 contributions: reset noise and integration noise [5].

1) Reset noise

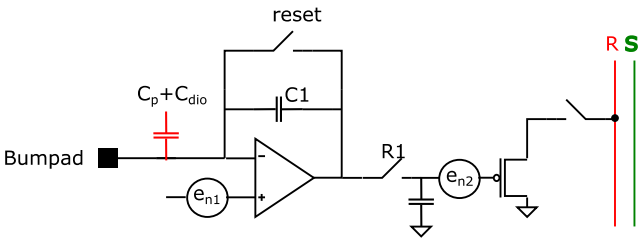


Figure 4: Simplified pixel schematic with dominant noise sources

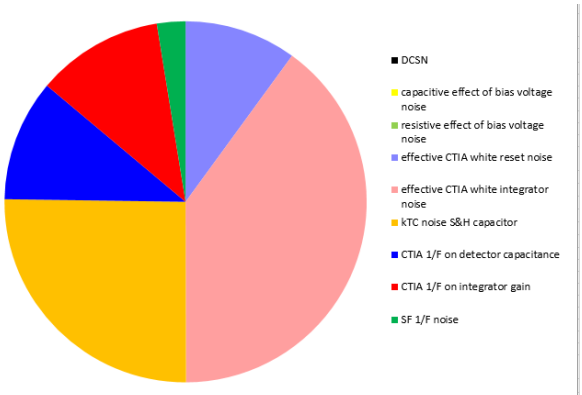
When the reset switch and R1 are toggled, the amplifier noise (represented here as e_{n1}) is sampled on the S&H capacitance. The noise is partly flicker noise of the amplifier and partly thermal noise. The noise is also sampled on the virtual ground node to an amount related to the total capacitance on that node. In practice, this node capacitance is thought of as C_p (parasitic capacitance) + C_{dio} (detector capacitance). For a ROIC without detector C_{dio} = 0.

2) Integration noise

After integration, the signal at the output of the CTIA is sampled on the signal sampling capacitor. The noise sampled in this phase consists of the amplified noise (e_{n1}) [gain=$(C_p+C_{dio}+C_1)/C_1$] and the amplified reset noise [gain= $(C_p+C_{dio})/C_1$].

When the signal value is subtracted from reset value through the in-column CDS operator, the thermal noise components are square-summed whereas the correlated noise (sampled reset noise from virtual ground node) is cancelled.

The overall noise contributions from different sources are shown in Figure 5. The pixel noise at the detector node is about 26 e-RMS. The thermal noise component scales down with the temperature, hence the noise at cryogenic temperature is lower than room temperature. Similar calculations show that the ROIC only noise at 77K is 15 e-RMS.



CDS **Applied**				CVFout [V/e]
BREAKDOWN				3.11E-05
noise source	CVF	at source [V]	Eq Detecto	eq Output [V]
DCSN			**0.0**	0.00E+00
capacitive effect of bias voltage noise			**0.0**	0.00E+00
resistive effect of bias voltage noise			**0.0**	0.00E+00
effective CTIA white reset noise	1.82E-05	**9.31E-05**	5.1	1.59E-04
effective CTIA white integrator noise	1.82E-05	**3.72E-04**	20.4	6.35E-04
kTC noise S&H capacitor	1.82E-05	**2.35E-04**	12.9	4.02E-04
CTIA 1/F on detector capacitance			5.6	1.73E-04
CTIA 1/F on integrator gain	1.82E-05	**1.05E-04**	5.8	1.80E-04
SF 1/F noise	1.82E-05	**2.37E-05**	1.3	4.06E-05
total noise			**26.0**	**8.09E-04**

Figure 5: All noise contributions, nominal operation

Pixel layout

It is known as one of the effect that when transistors are exposed to radiation, charges are trapped in the shallow trench isolation (STI) and form a channel from drain to source of the transistor underneath STI. The channel causes a leakage current between drain and source of transistor resulting in increased power consumption and loss of signals levels. The radiation damage can be mitigated by techniques like enclosed transistor layout and H-gate transistor layout [6].

The H-gate transistor layout technique is followed in the layout of this ROIC because it is compact compared to enclosed transistor of similar sizes and the layout extraction of enclosed transistor is difficult for verification.

The layout snapshot of a 2x2 pixel arrangement is shown in the Figure 6. The location of amplifier and source followers are indicated in the layout. Only the active area, poly and metal 1 are shown. The 2x2 layout of Top metal (M6) and MIM capacitors are shown in Figure 7. The MIM S&H capacitors are implemented as double MIM between M4-M5-M6 of 150 fF each.

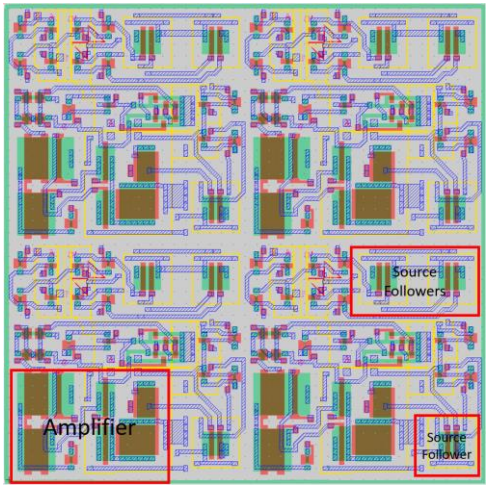


Figure 6: 2x2 pixel layout of BOL layers

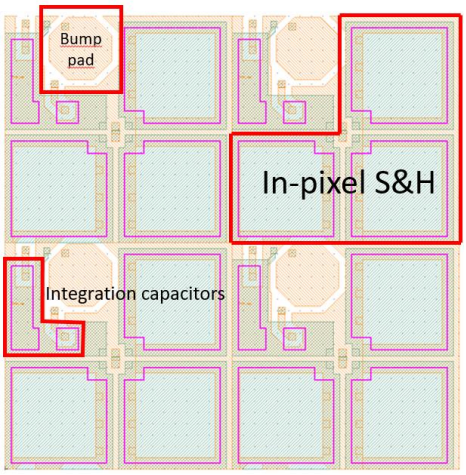


Figure 7: 2x2 layout of Top metal and MIM capacitors

Parasitic extraction

The dense pixel layout results in an unwanted coupling between different nodes of the pixels or even between neighbouring pixels [7]. It is foreseen that the coupling capacitance is less than 1% of the node capacitance. The parasitic extraction was done on a small array of 3x3 to study the coupling capacitance is shown in Figure 8.

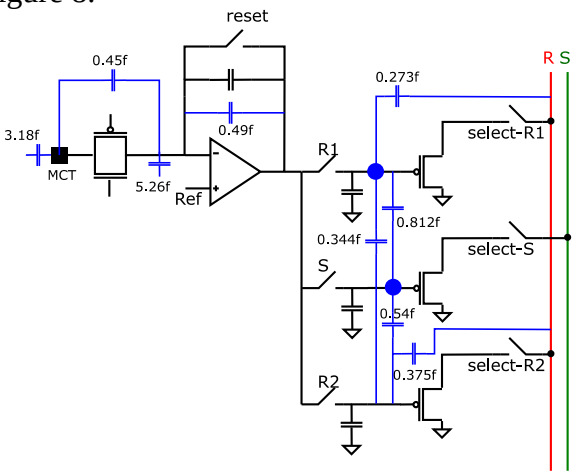


Figure 8: Extracted parasitic capacitors

The ROIC is and should be insensitive to visible light. The functionality of the pixels without detectors can only be measured by injecting a current at the detector node through a resistor or capacitor in certain test pixels as shown in Figure 9.

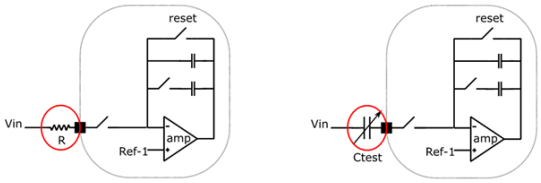


Figure 9: Test pixels

The pixels in the topmost row are test pixels and are provided with on-chip resistive and capacitive inputs.

The pixels with resistive input saturate depending on the voltage 'V_{in}' w.r.t reference voltage 'Ref-1'. If V_{in} > 'Ref-1' then the output of amplifier saturates to VSS while it saturates to VDD if V_{in} < 'Ref-1'.

The pixels with capacitive input shows responses depending on the ΔV change on 'V_{in}', the value of the capacitor 'C_{test}' and integration capacitor (C_{int}).

$$Output = \Delta V * C_{test}/C_{int}$$

Measurement results

The ROIC is tested at room temperature without bonding the detectors.

1) Laser Illumination

The ROIC is light insensitive. However, due to the diodes at the source and drain of the switches at the virtual ground the ROIC is sensitive to high illumination. A laser line is shined across the sensor and images are captured. This test serves to prove the working of the peripheral and driving circuits.

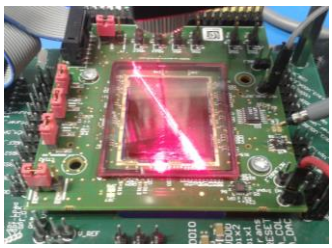


Figure 10: Test setup

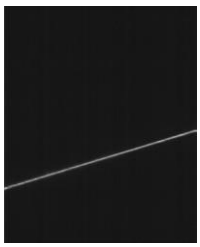


Figure 11: Captured image

2) Testpixel measurements

As described above, the pixel with capacitive input is used to measure the response of the pixels. The measurement results are shown in Figure 12. The input capacitor 'C_{test}' are designed to have 8 fF, 32 fF, 64 fF, 128 fF,256 fF, 512 fF. The input voltage is changed in varying steps and the output is plotted. It can be seen from the plot that pixel responds linearly over the entire range.

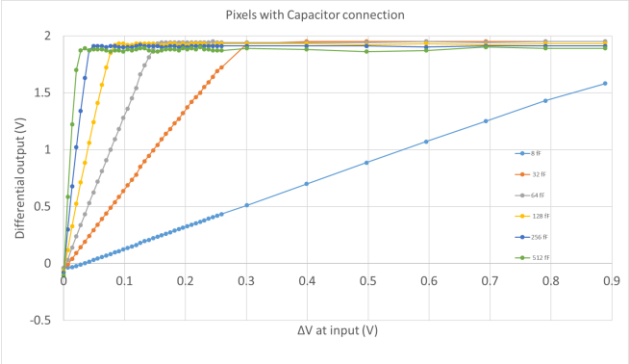


Figure 12: Capacitive input test pixels measurement

3) Noise measurement

The noise measurements of pixels always in reset and under nominal operation in ITR readout mode is shown in Figure 13. The measured noise of the pixels in reset is between 24 to 32e^-_{RMS} and under nominal operation it is between 30 to 42e^-_{RMS}. It was predicted to be 26e^-_{RMS} under nominal operation. At 77K these values will drop to about 15-20e^-_{RMS}.

The higher noise than the prediction is because the noise contributions from the downstream electronics (column S&H, column amplifier and output amplifier) is not considered in calculations. The useful output voltage range is 0.5V-2.5V (supply=3.6 V) at cryogenic temperature.

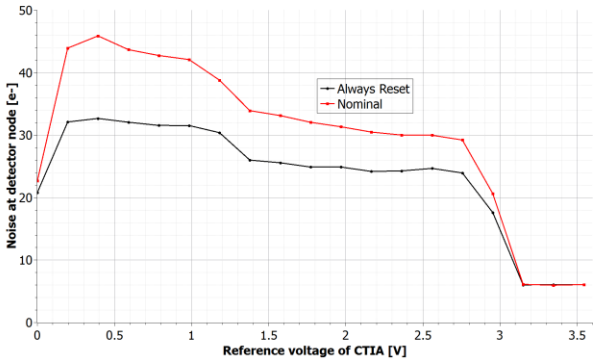


Figure 13: Noise in e- at detector node vs reference voltage

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