Rad-hard image sensors area/power/hardening trade-offs

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Outline

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- Motivation
- A short summary of radiation effects
- A short summary of counter measures
- Countermeasure effect on area, speed and power
- Take home messages

Chapter 1
MOTIVATION

Purpose

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- Overview of actual radiation hard circuits
- Direct comparison with the non-radhard equivalents.
- For image sensors and their periphery circuits.
- Focus on different type of radhardness and their impact on area, speed and power

- *Not* touch the actual hardness levels achieved nor pixel radhard design

Example

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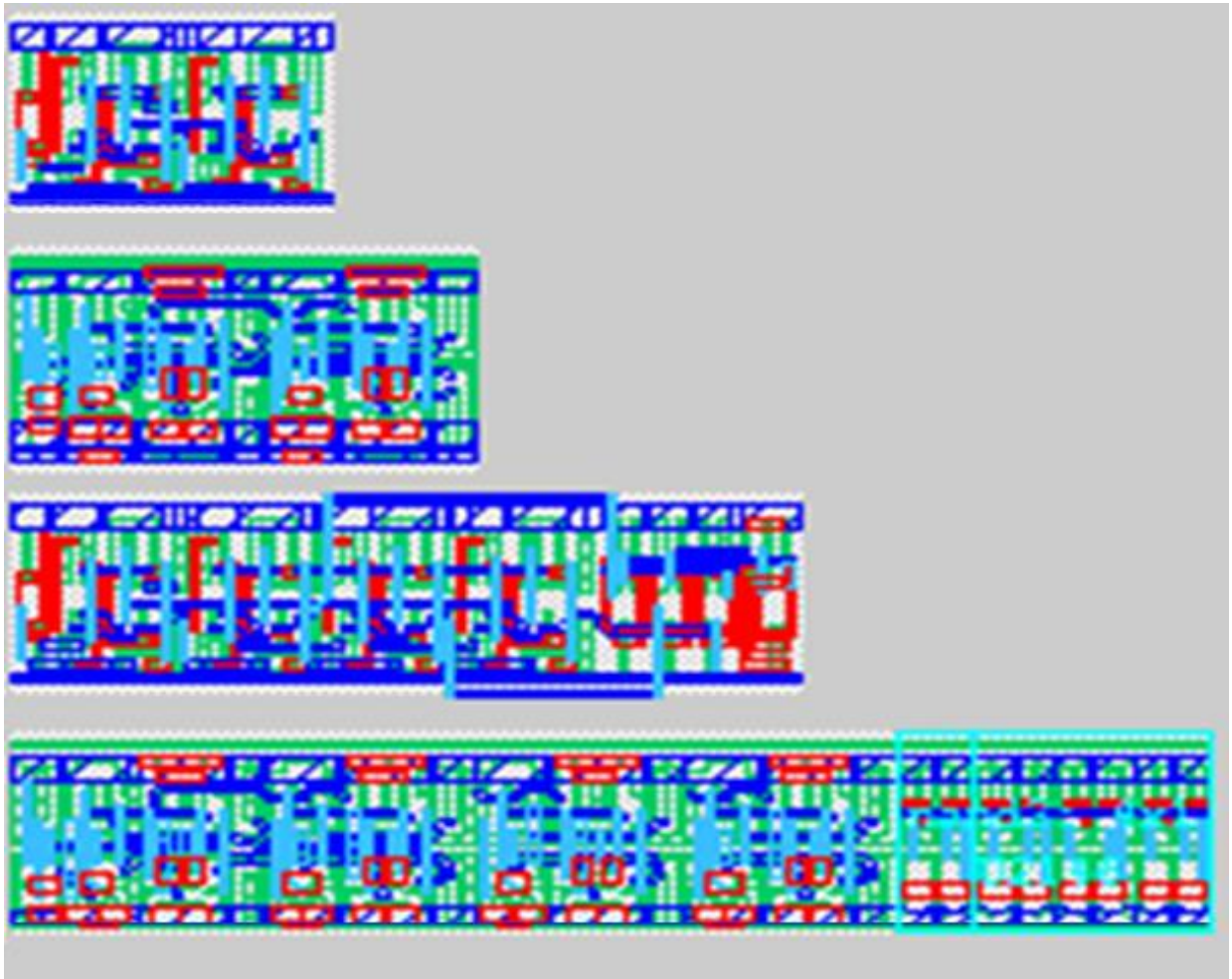
A common logic block: different level of radiation hardness.
As each of these are different in approach and effect, this is rather a case study than a systematic overview.



Non-radhard

TID+SEL hard

SEU+SEL hard (TR)

Both combined

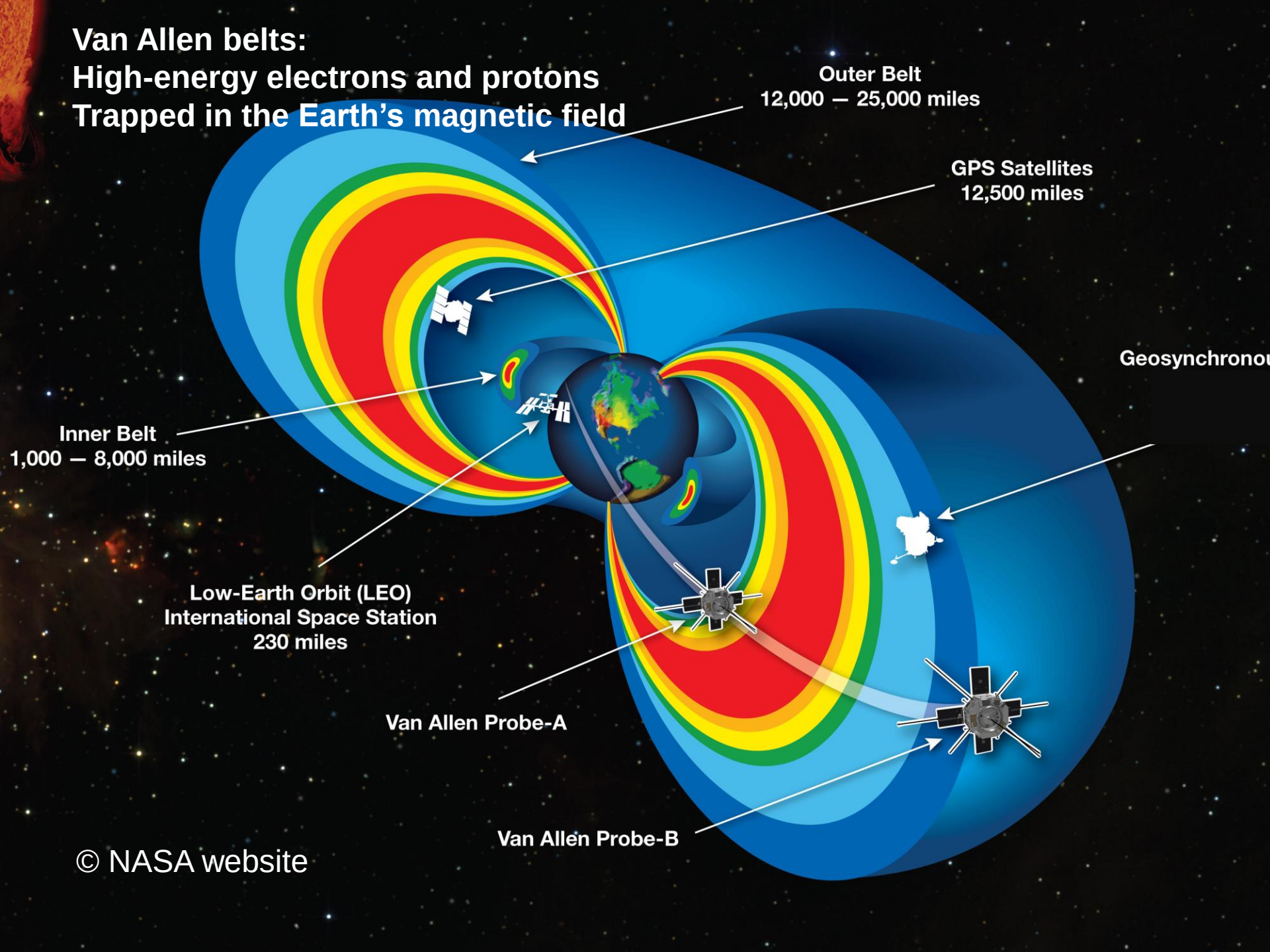
SE hard and not TID hard?

It is perfectly possible – and this actually makes sense – to design purely for SEL (single event latch-up) hardness, and disregards the other forms of hardness.

SEL hardness usually does not require a large area penalty in image sensors, whereas for many mission types it is the only damage mechanism that may be threatening for the mission.

Chapter 2

SHORT SUMMARY OF RADIATION EFFECTS


Van Allen belts:
High-energy electrons and protons
Trapped in the Earth's magnetic field
Outer Belt
12,000 — 25,000 miles
GPS Satellites
12,500 miles
Geosynchronou
Inner Belt
1,000 — 8,000 miles
Low-Earth Orbit (LEO)
International Space Station
230 miles
Van Allen Probe-A
Van Allen Probe-B
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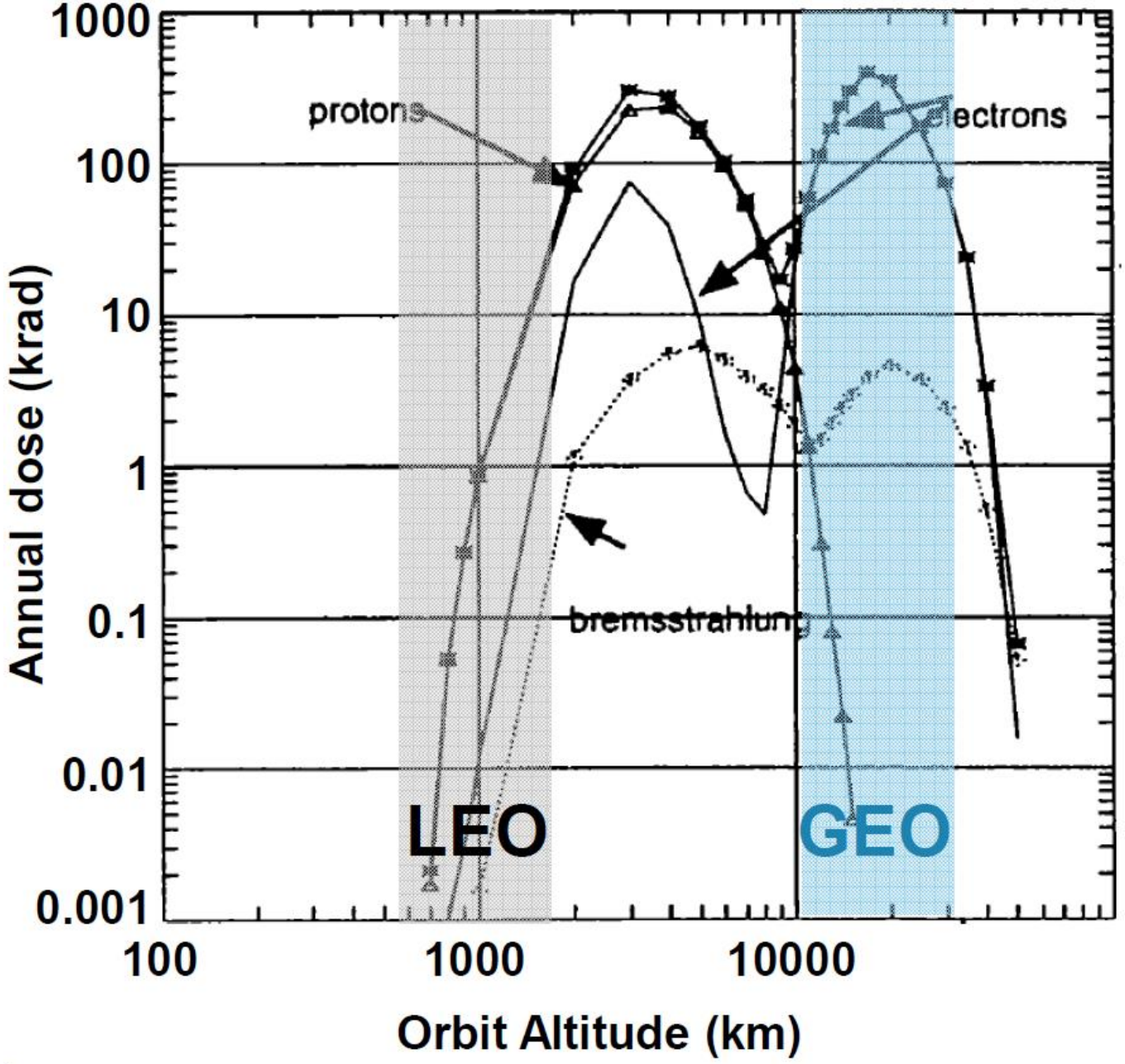

Space hazard	Total radiation dose	
Specific cause	Trapped radia-tion	Solar particle
LEO <60°		
LEO >60°		
MEO		
GPS		
GTO		
GEO		
HEO		
Inter-planetary		

Important

Relevant

Not applicable

From: V.Huard, “Enabling space applications in advanced CMOS nodes: challenges and oportunities”, March 1, 2016

SEE(Single event effects)

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- SEU single event upset
- SEL single event latch-up

There exist many more “SE”s, such as SEGR

- Which are typically rare or irrelevant in CMOS
- Have no countermeasure except shielding or the SEU/SEL counter measures already in place

SEU

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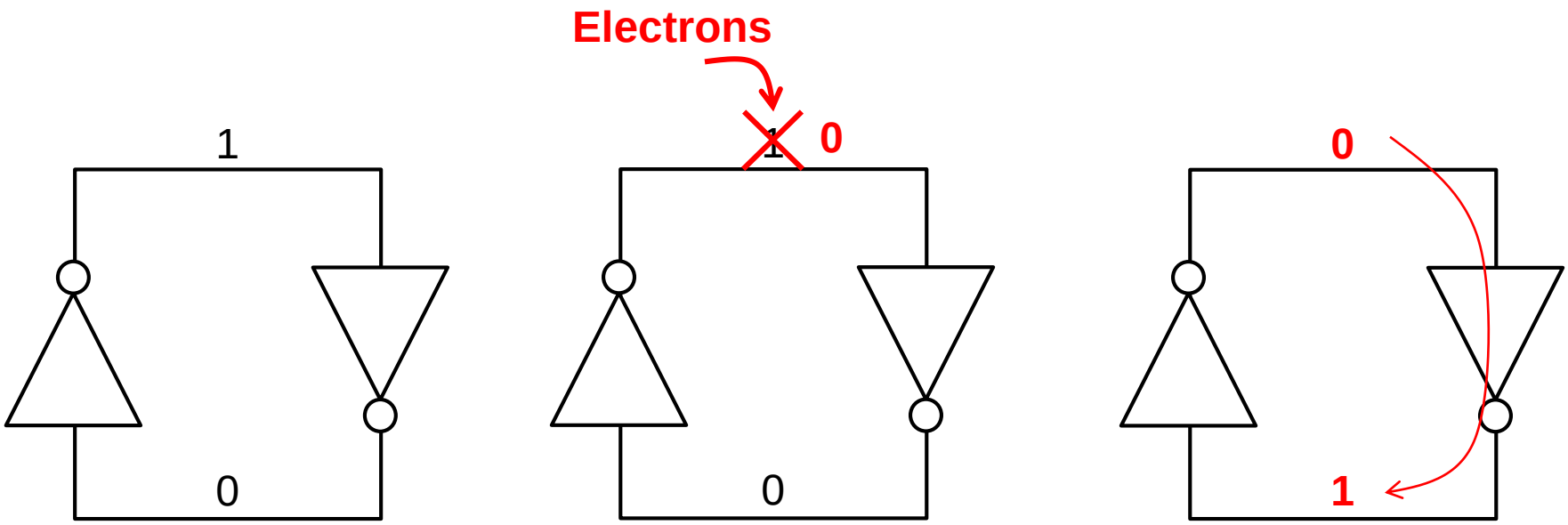
Corruption of bit in SRAM or Flip-flop

⇒Charge packet deposited by particle charges

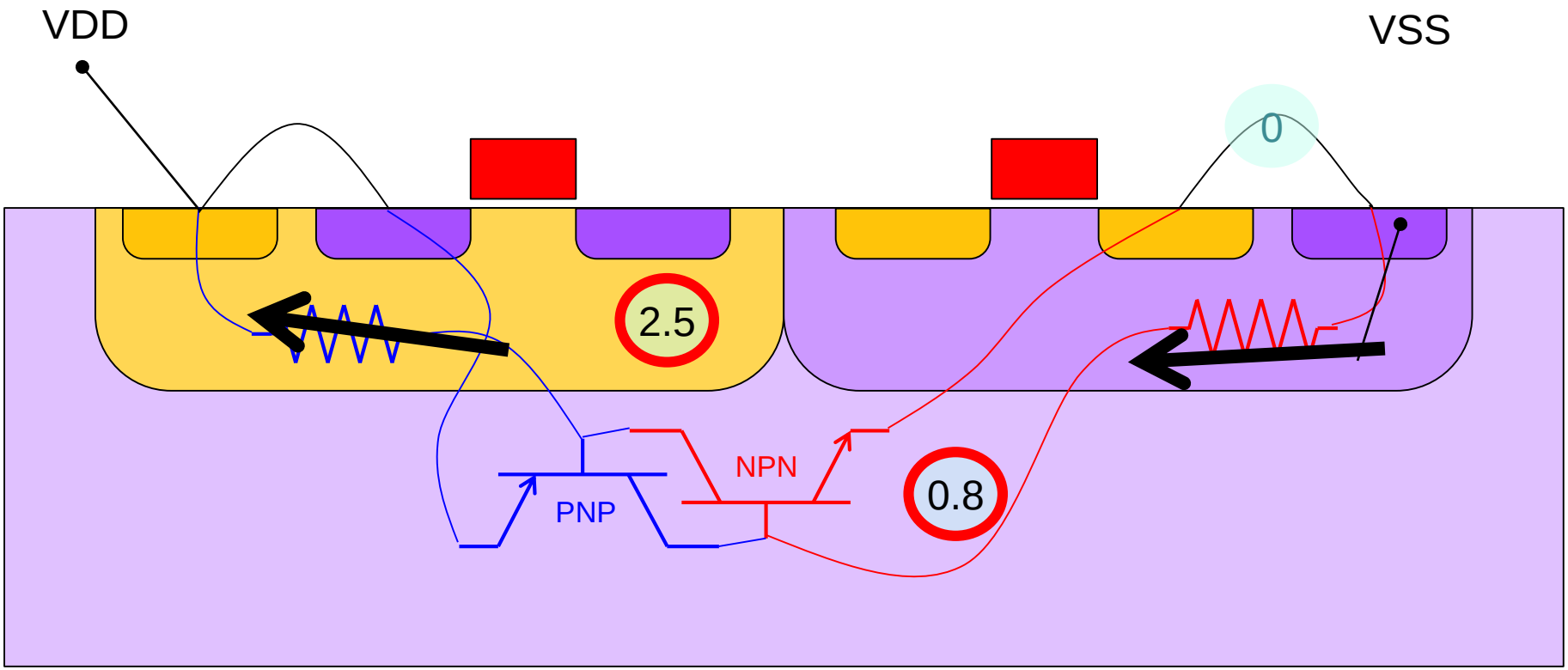
⇒One node of a latch to the opposite logic value



SEL

High energy particals tuned on the parasitc thyristor of bulk silicon

⇒power supply shorts



TID (total ionizing dose)

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Radiation:

⇒X, γ ,charged particles

Dominant effect :

⇒Positive space charge in dielectric layers

⇒Increase of interface states at Si-SiO_2

Effect on CMOS circuits:

⇒ Moderate degradation of Vth, μ and 1/f noise

⇒ Parasitic S-D leakage in nMOSFETs

Chapter 3

SHORT SUMMARY OF COUNTER MEASURES

TID-hard nMOSFET

avoid the parasitic S-D leakage

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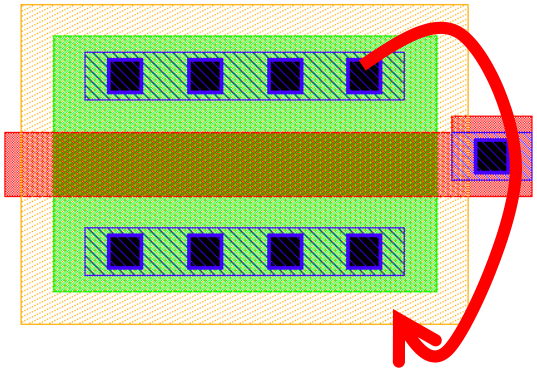
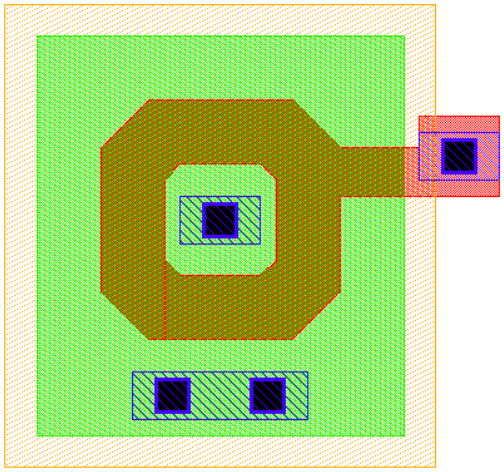
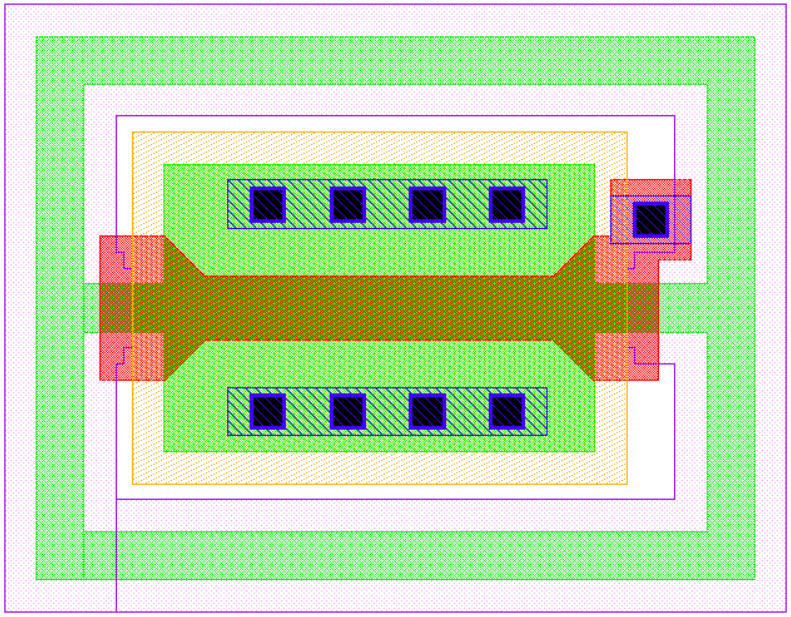


Regular transistor

Leaks when STI/field inverts due to positive charge built-up due to ionizing radiation

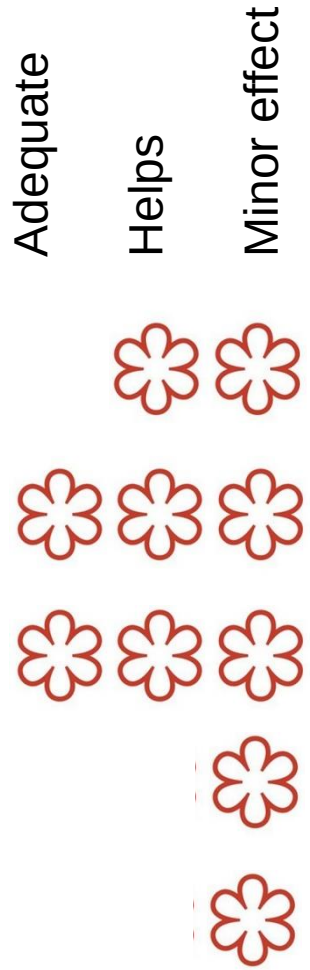


Annular transistor:
No path over STI/field



H-gate transistor:
Leakage path over STI/field is blocked by P-implant

TID countermeasures



- Shield against radiation
- Ring MOSFETs
- H MOSFETs
- SOI/FINFET
- Defensive circuit design

SEU

Design countermeasures using TR

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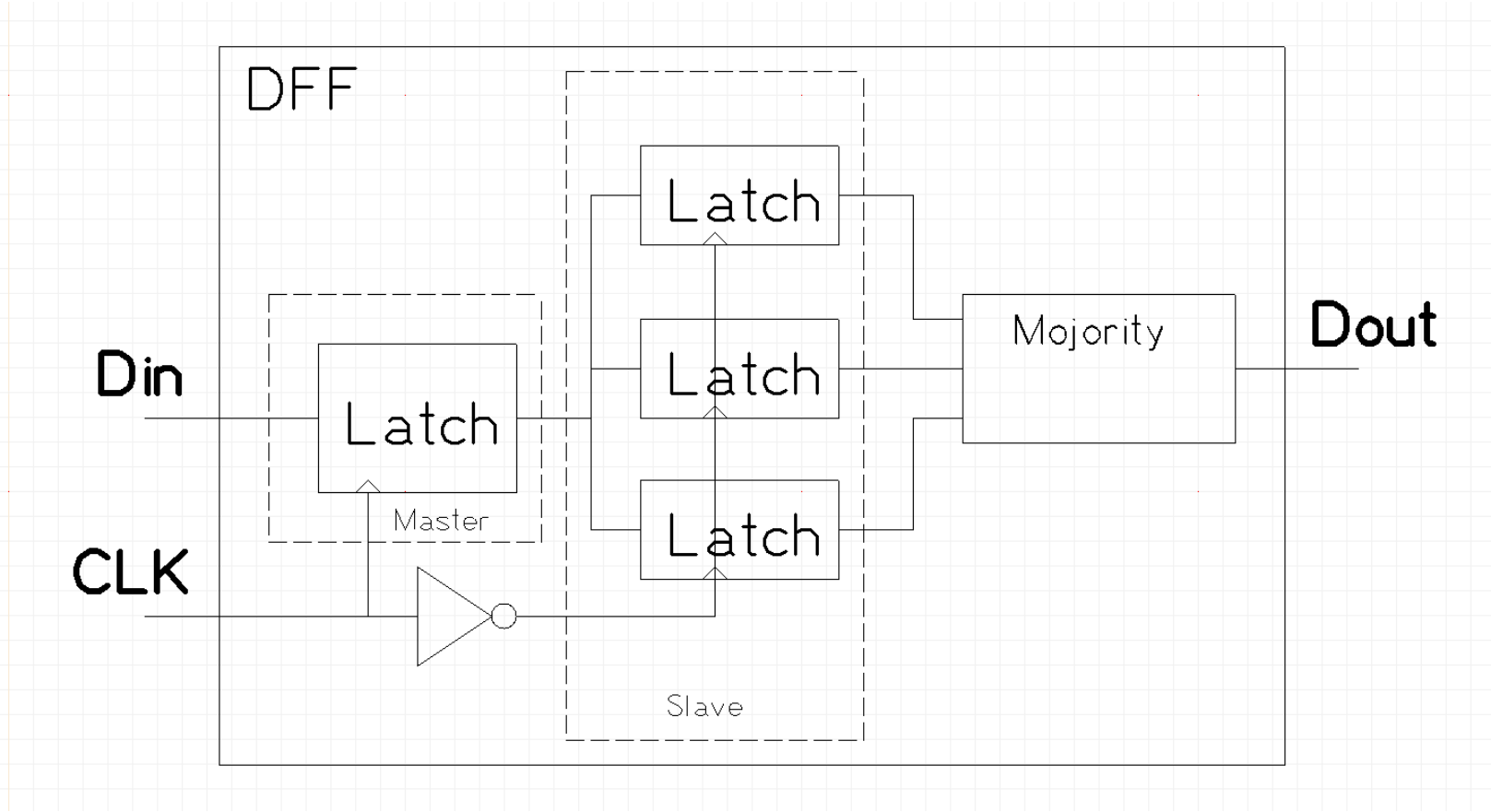
Triple-redundant-slave flipflop



SEU countermeasures

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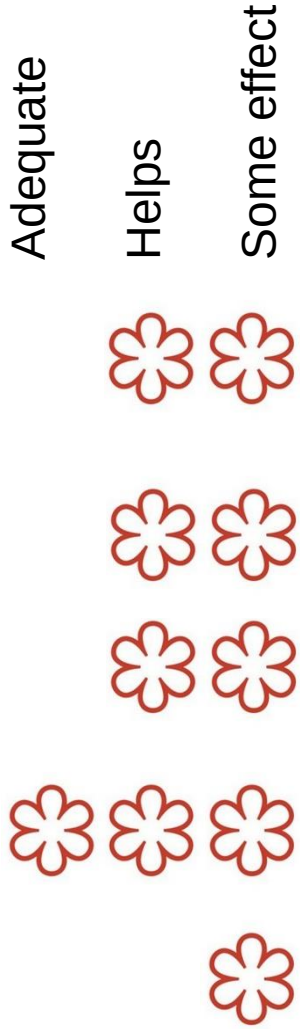
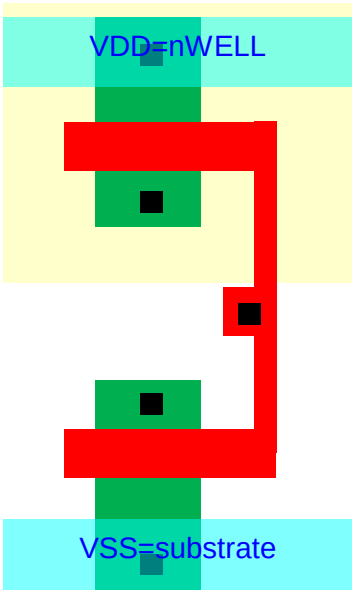


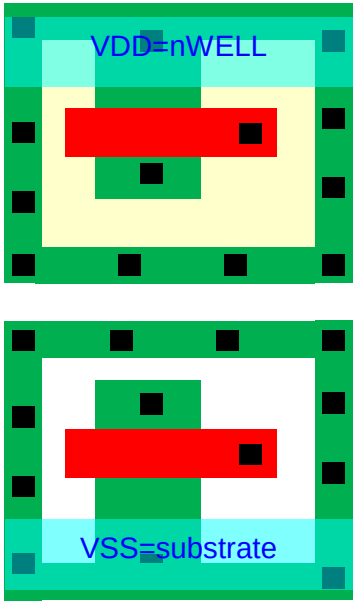
SEL

Design counter measures using guard rings

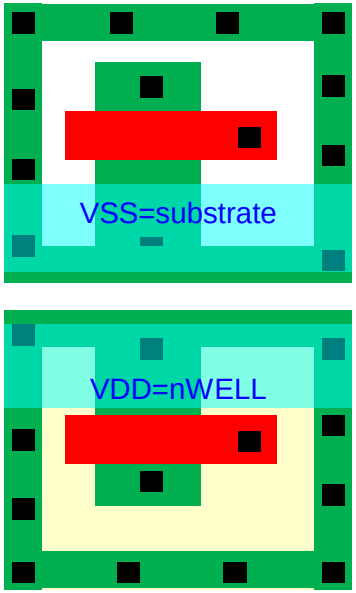
Classic CMOS design style



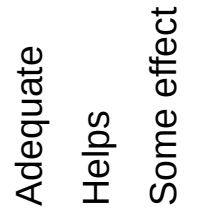
Metal guardring around wells



Rails in the middle



SEL countermeasures



Avoid ignition

- ⇒ Reduce pick-up: minimize sensitive volume
- ⇒ maximize C/Q: increase node capacitances
- ⇒ No thyristor: SOI, nMOS only, FINFET

Avoid sustaining

- ⇒ Reduce the series resistance in the thyristor
- ⇒ guard rings metallically tied to VDD/VSS

Avoid proliferation

- ⇒ Fragment nWELLs
- ⇒ Detect & reboot

Chapter 4

LAYOUT EXAMPLES

(A)SPI register

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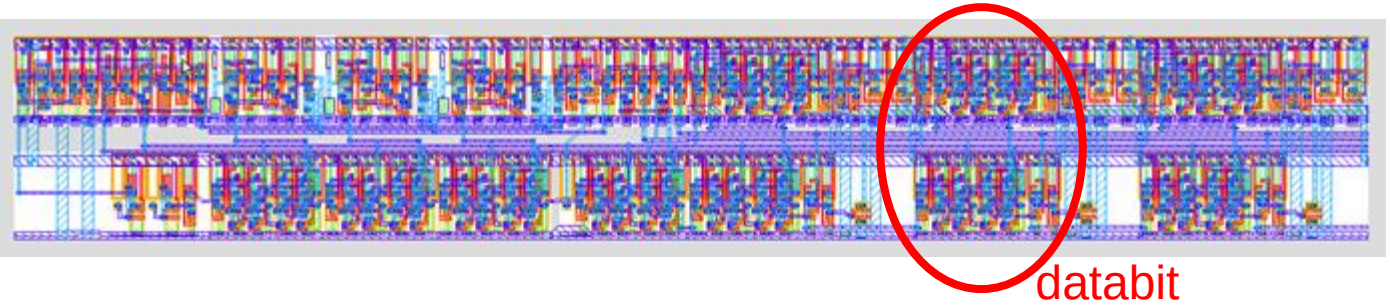
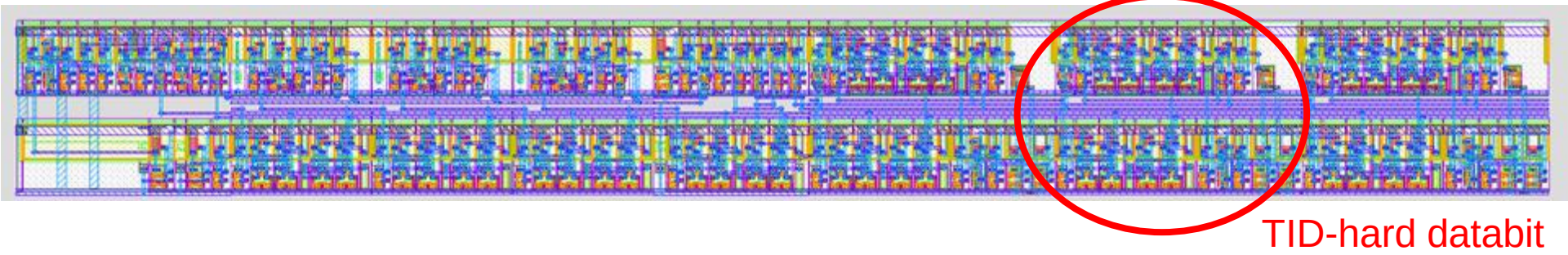
normal

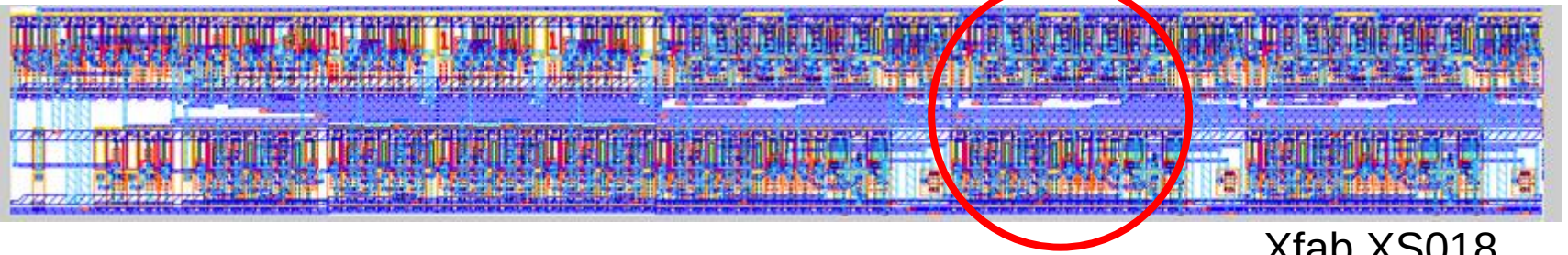


Static register with (here)
- 3 address bits
- 3 databits

TID-hard, SEL-hard



SEU-hard by TR data register, SEL-hard, not TID-hard



IO rail RDAC

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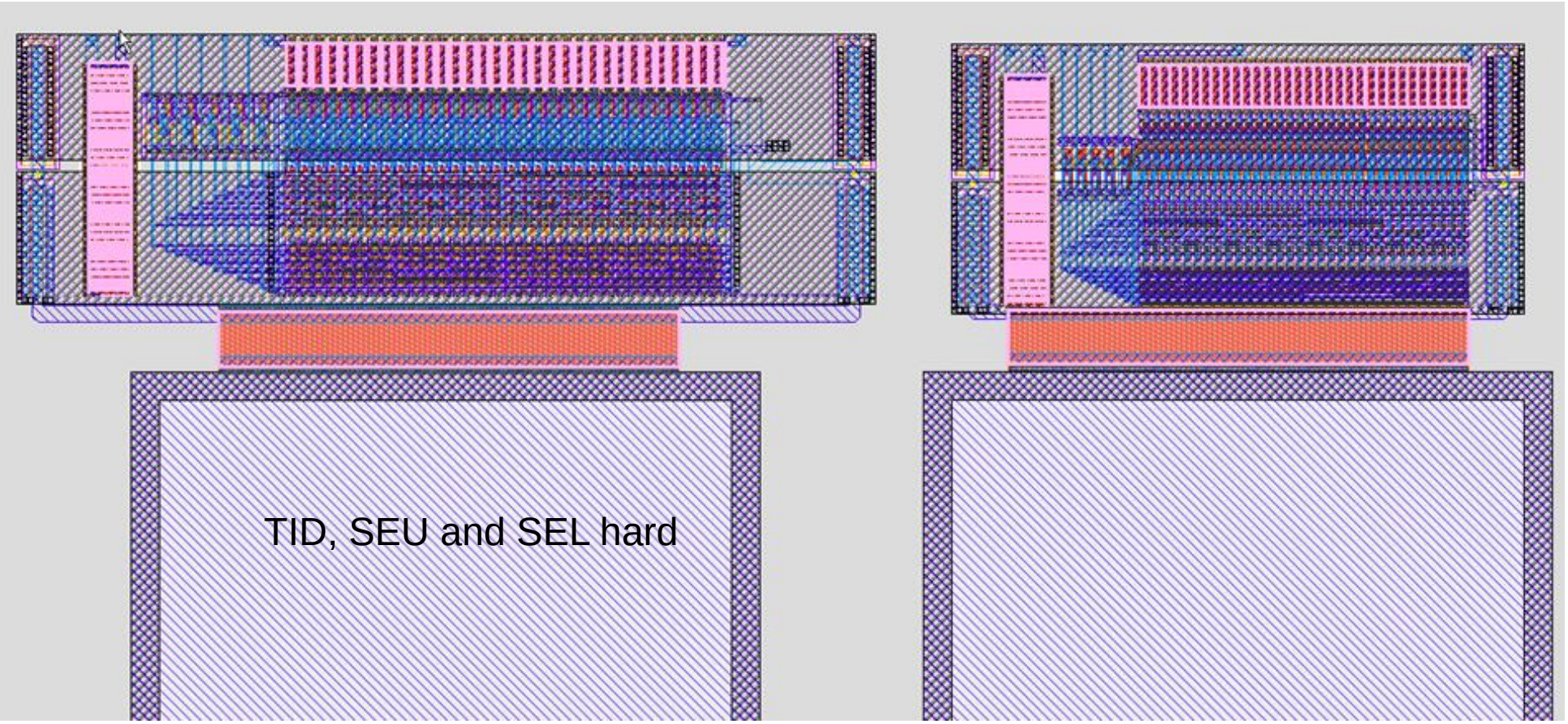

IO rail programmable bias

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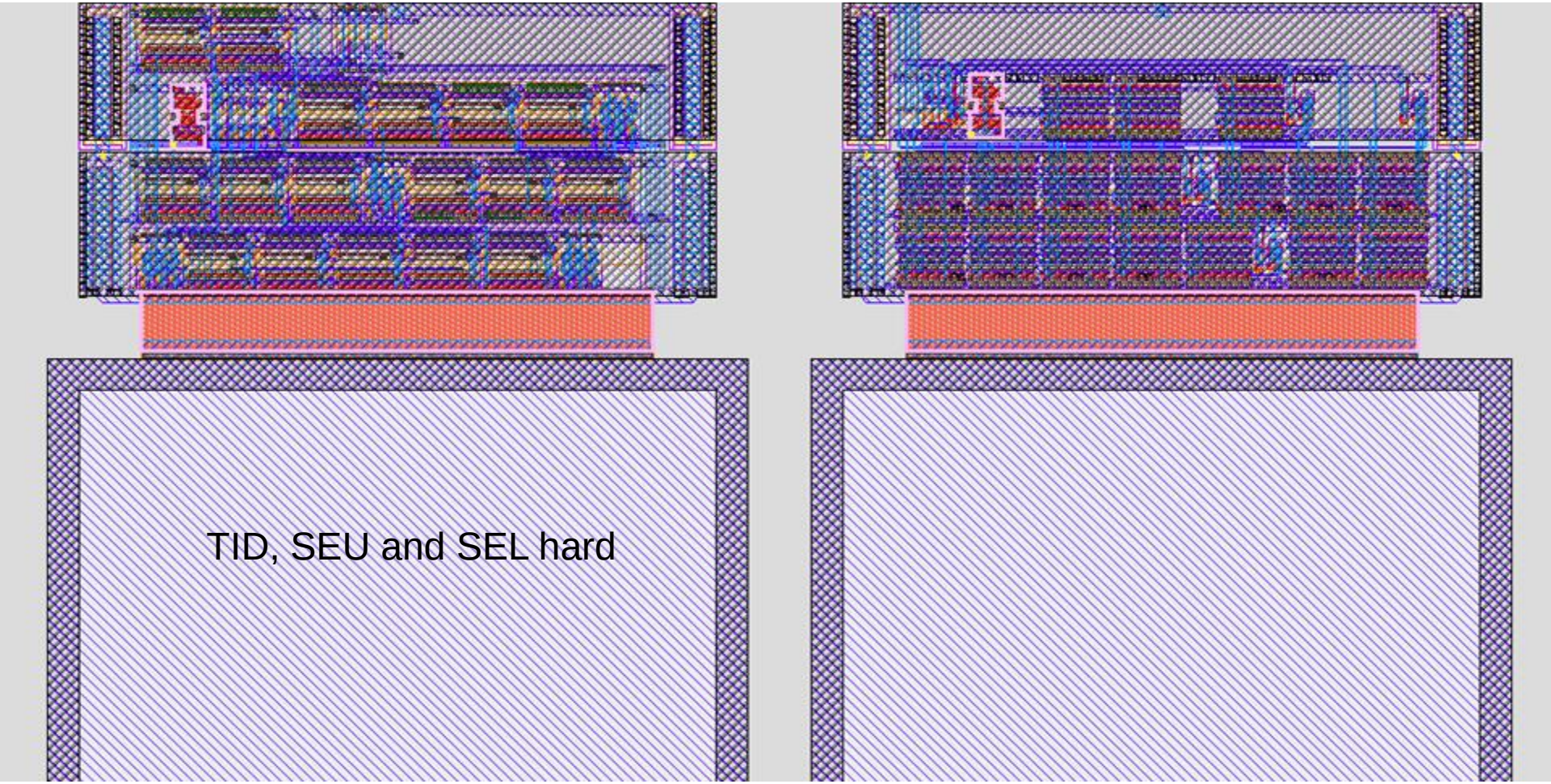

IO analog buffer

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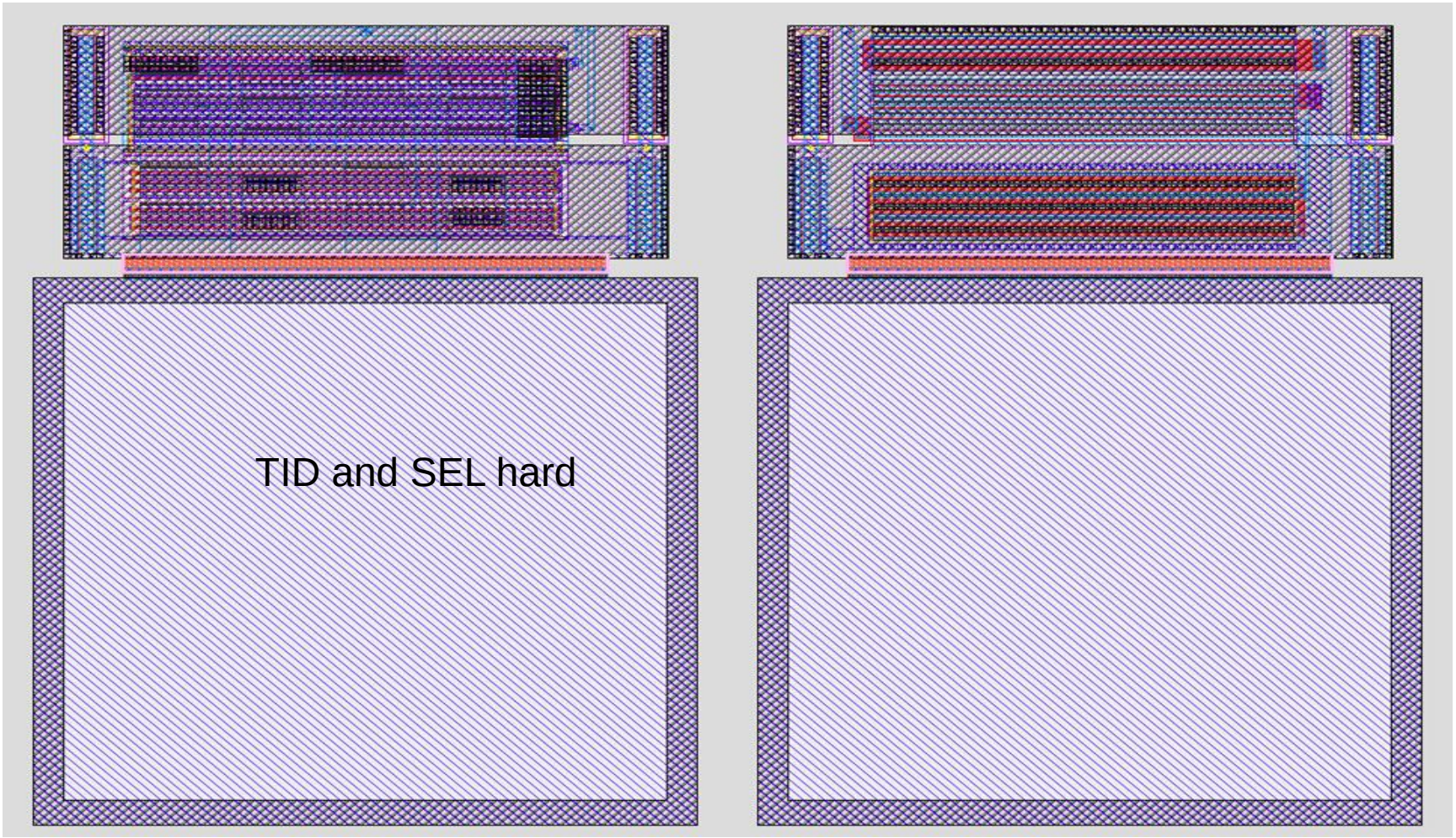
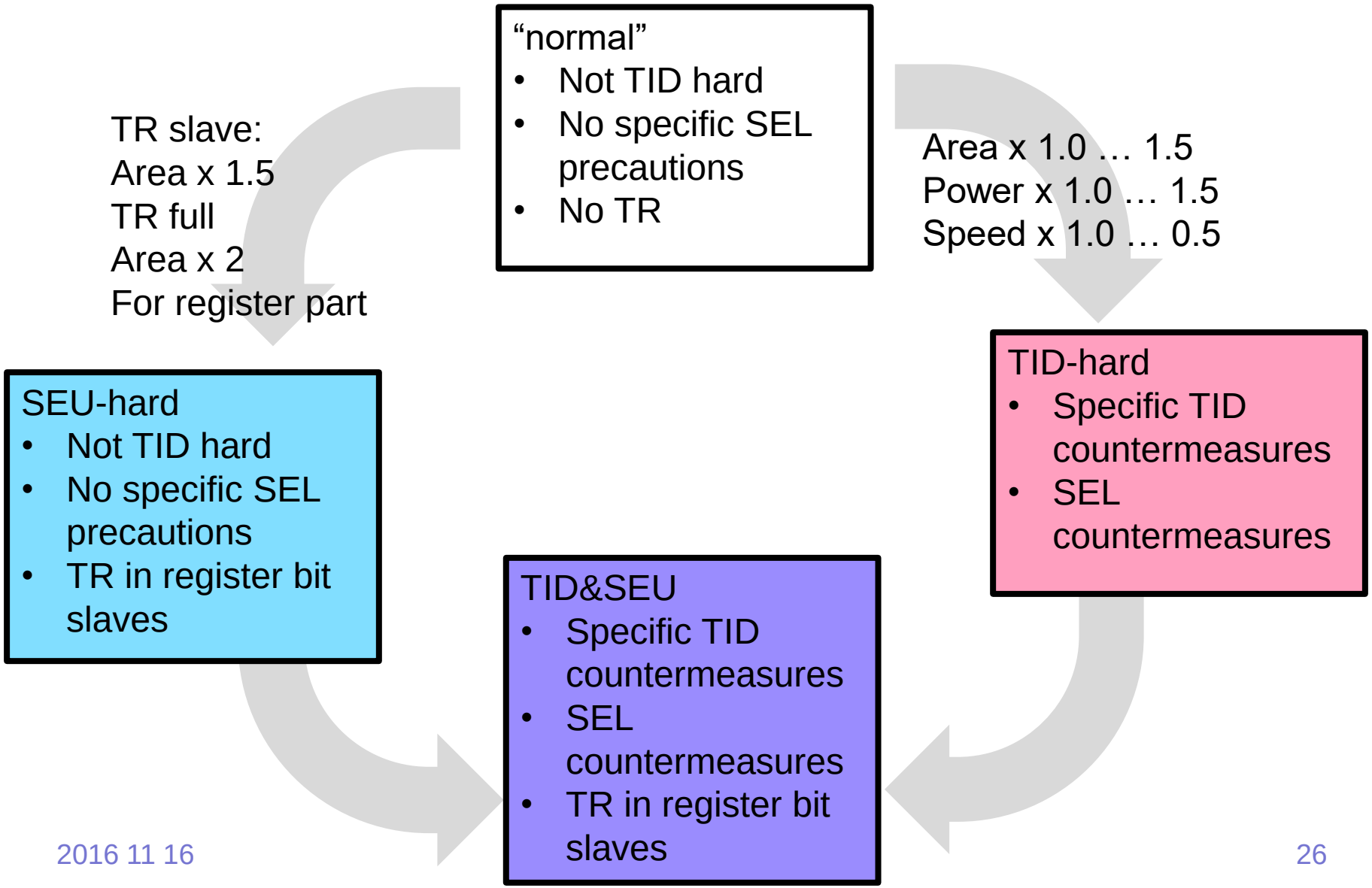


Cost of hardening



Chapter 5

TAKE HOME MESSAGE

Take home message

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Total Dose (Ionizing and Displacement damage)

- ⇒ High radiation hardness can be designed for
- ⇒ Weak points remains I_{dark}

Single Events(mainly SEU and SEL)

- ⇒ Nearly perfect protection against SEU and SEL can be designed for.
- ⇒ Remains weak for: very heavy ions
- ⇒ Inherent weak point: the pixel itself is made to detect radiation.

Independent TID and SEE hardness

- ⇒ Can be independent implemented.
- ⇒ Trade off depends on mission type, duration, shielding conditions, FEE intelligence...

References

- V.Huard, “Enabling space applications in advanced CMOS nodes: challenges and oportunities”, March 1, 2016

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Thank you!