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CAMPANION2: ASIC for Large Format Detectors

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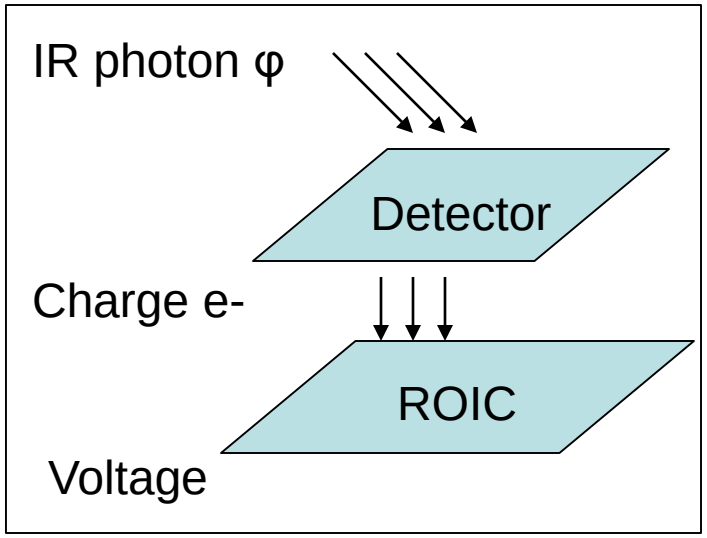
Caeleste, Belgium; *EASICS, Belgium; **SRON, Netherland; ***ESTEC, Netherland; ****ONERA, France

Outline

- Introduction
- CAMPANION2 overview
- Design of the key building blocks
  - Regulator
  - Analog paths
  - Others
- Take home message

Introduction



The signal chain from radiation detection to digital

Image out (V)

Parallel

CLK/biasing/power in

FEE (Front end electronic)

Image out (D)

Serial

Power/ Control data in

Computer

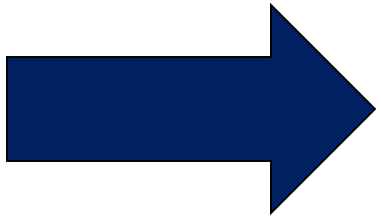
Analog domain

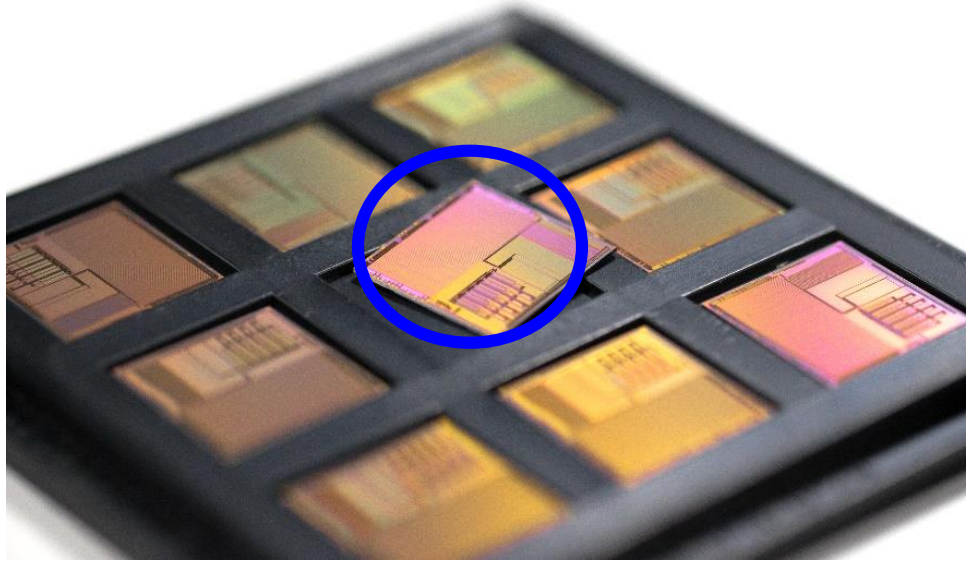
- Signal conditioning
- A/D converter
- Regulated power supply
- Bias voltage/current references
- House keeping

Digital domain

- Sequencer
- Memory
- Data Communication

Introduction

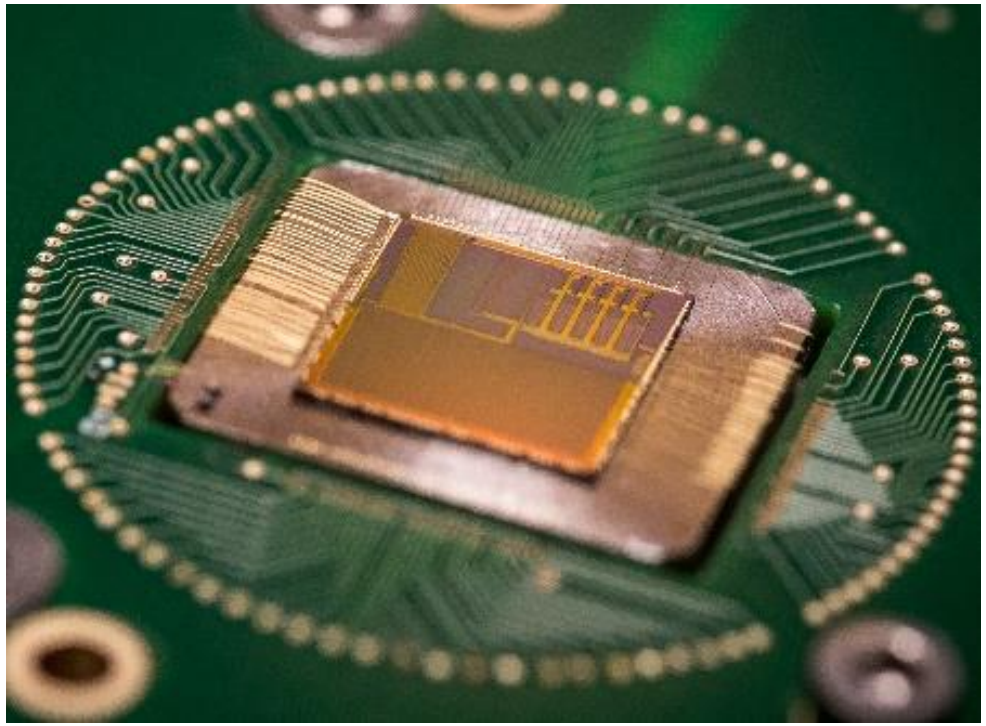




[Z.Zhao.SDA'05]

In-house heritage

“CAMPANION 1” (2012 prototype)



- Analog blocks:
  - Data acquisition: PGA + ADC
  - Ref. DAC
  - LDO
- Digital block
  - On-chip programmable sequencer
- Cryogenic operation
  - Full functionality demonstrated at 77K
- Radiation hardness:
  - Digital: DARE180
  - Analog: Caeleste RH
- ADC INL/DNL issue limited the ADC to 12 bit
  - Signal dependent crosstalk inside comparator [Peng ICSO’2014]
- Highly flexible control for ROICs

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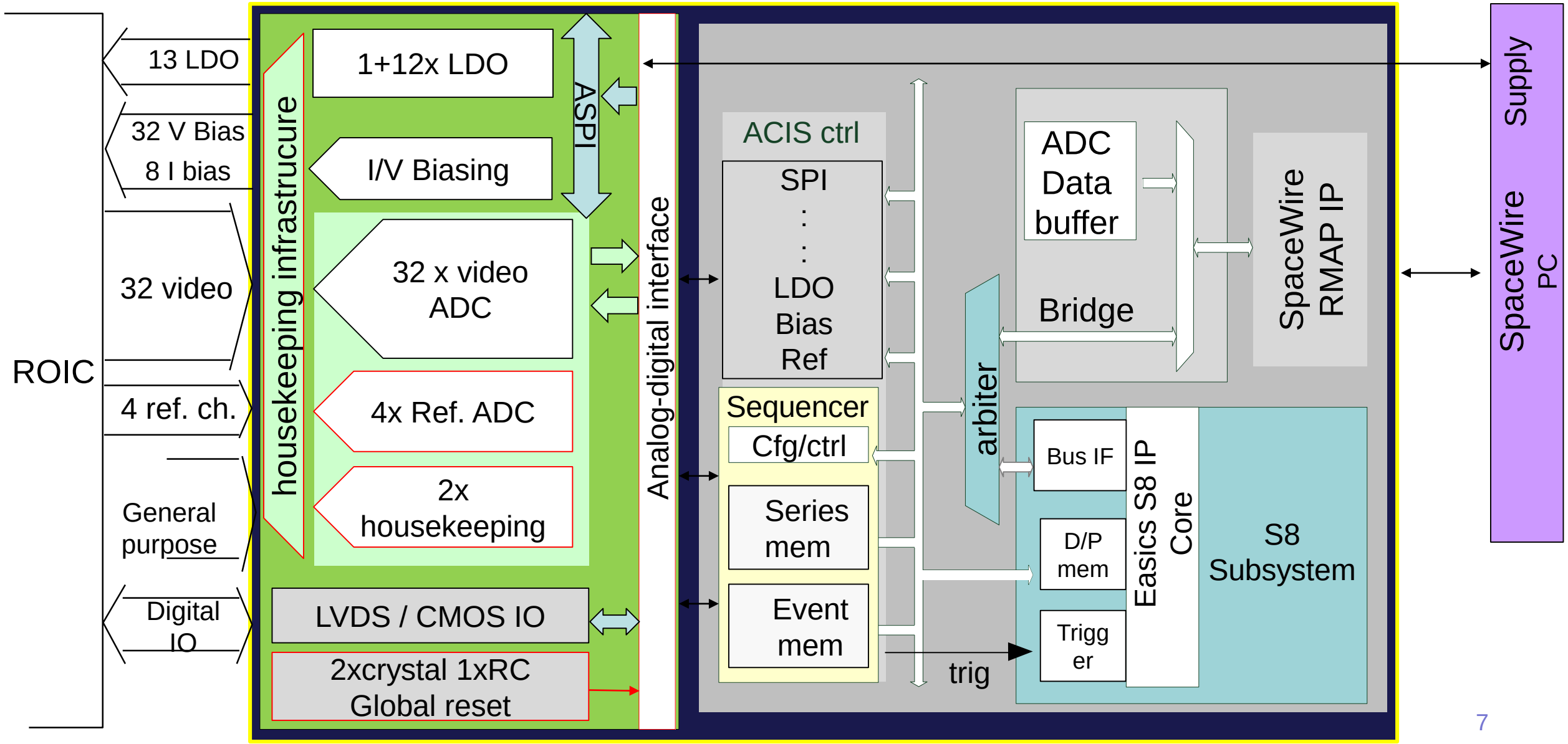
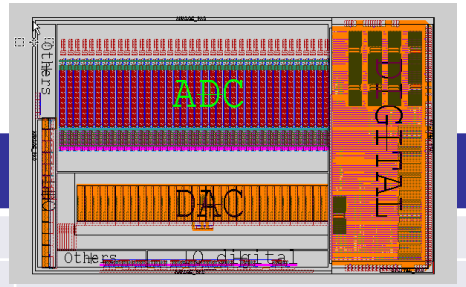
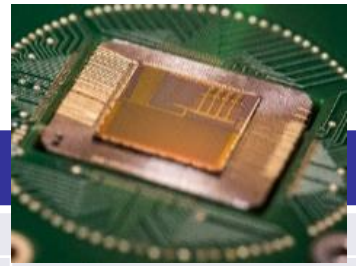
Campanion 2 floorplan



Campanion 2 features





	Function	CAMPANION2		CAMPANION1
ANALOG(CAELESTE)	LDO	13	1-3.4V programmable 10bit	4	1.1 -3.4V programmble 6bit
	Video channel	32	Single/diff & chopping	4	Single
	Reference channel	4		0	
	Channel biasing	Y	Prog. 10 bit R-2R DAC	Y	8 bit R ladder DAC
		Y	Prog. Current load	N	
	ROIC Reference	32	10 bit R ladder DAC	16	10 bit R ladder DAC
		8	Prog. Current DAC	0	
	ROIC housekeep	2	Internal/ external	4	External
DIGITAL(EASICS)	Master clock	4	Auto detect	1	External
	System protocol	Spacewire			
	ROIC digital control	32	Single / Diff. (LVDS) programmable between 1.8-3.3V	32	Single ended 3.3V logic
	ROIC inputs	16		8	
	ROIC programming	SPI			

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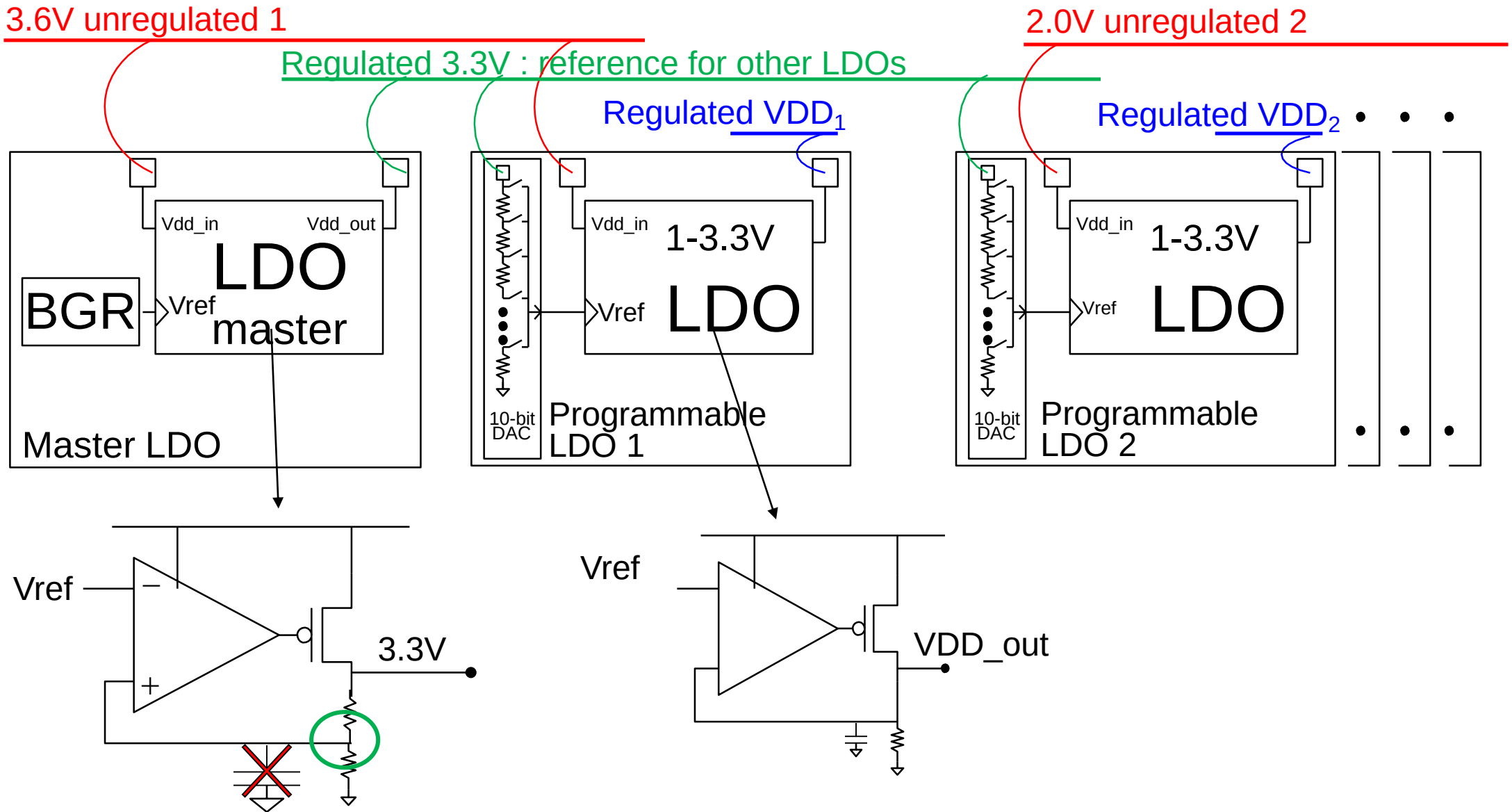
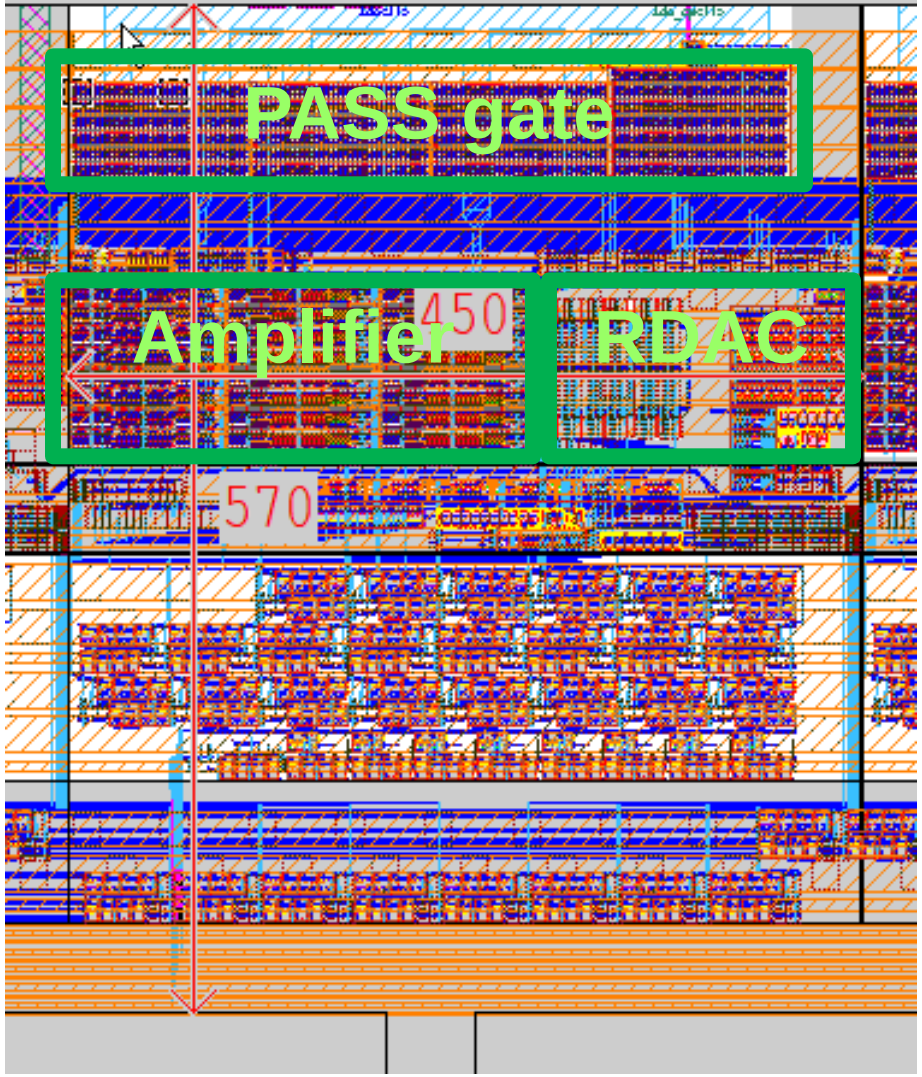
Regulator improve stability with fine programmability



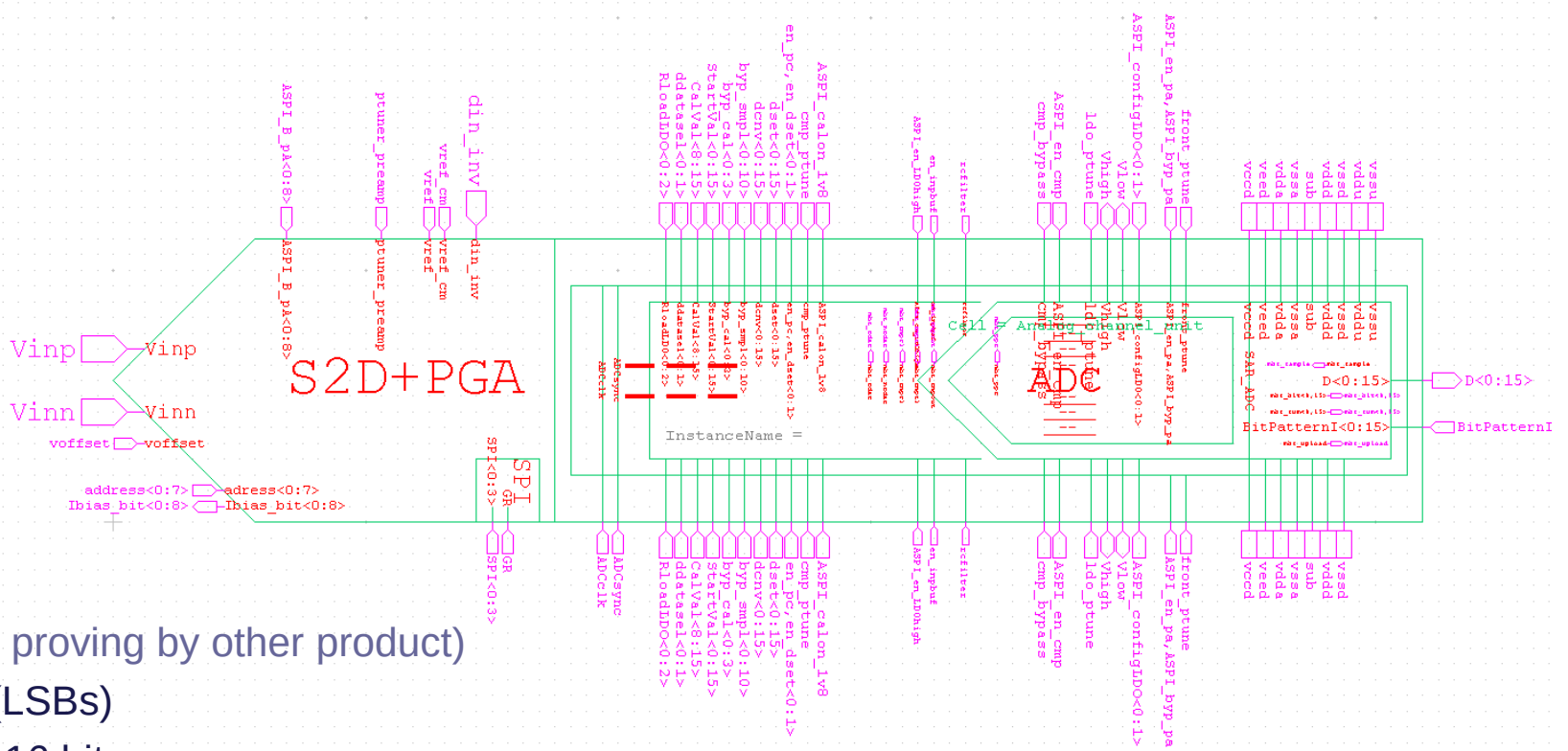
Regulator

Specs	value
Number of regulators	13
Output range	Key LDOs: 3.3/1.8V < ±10% Slaves: 1-3.4V (3mV step)
Current compliance	4 programmable levels 40mA, Master: no compliance
Max output current	40mA or no compliance
Output impedance	< 0.25 Ohm
Load capacitance	5 µF
PSRR	60dB
Noise	<40µV @3-300kHz

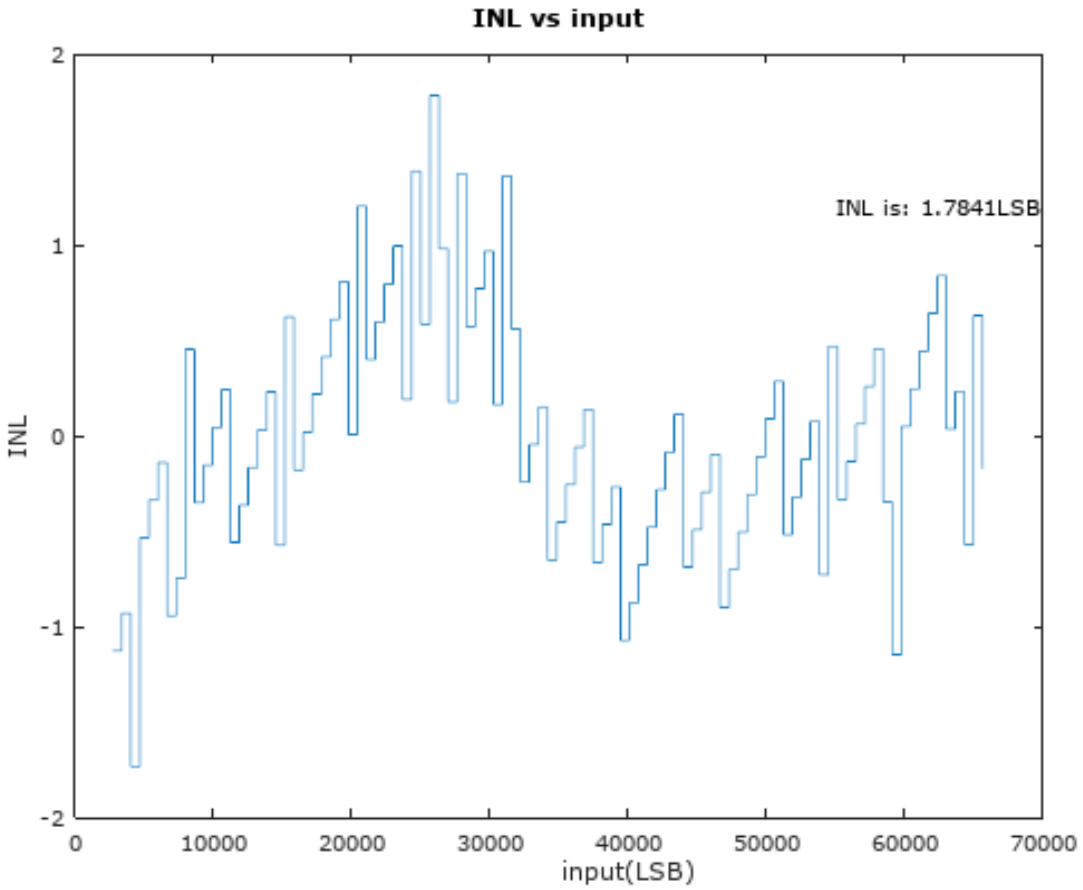


Video channel

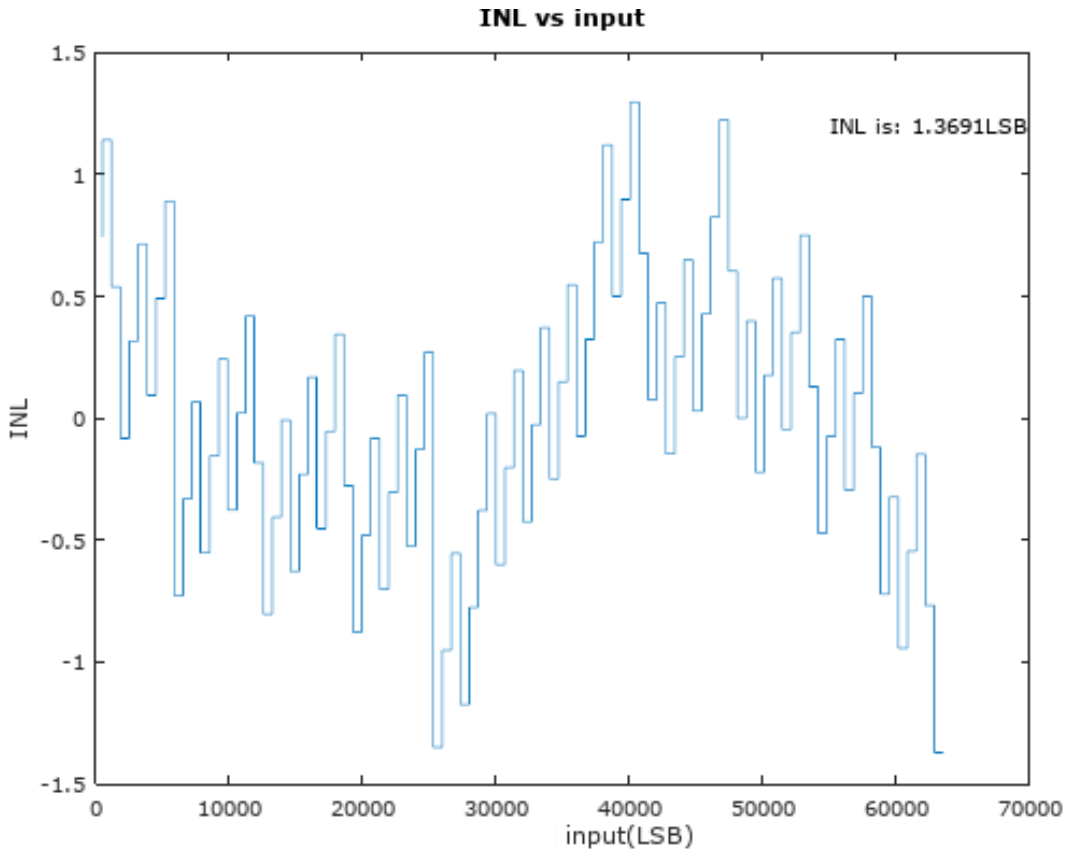
- Programmable PGA
  - 0dB-32dB in 3 dB step
- Programmable offset
  - 10-bit R2R DAC
- Programmable load current
  - Source or drain to the ROIC output
  - 10nA to 10mA per ch. prog.
- Sampling method
  - 32 Single ended
    - 64 single interleaved
  - Fully Differential
  - Chopping (CDS) at sampling rate
- New SAR ADC concept (concept silicon proving by other product)
  - DAC: Unary(MSBs), binary, R-DAC(LSBs)
  - More conversion cycles: 32 CLK for 16 bit
  - Possible post correct:
    - Reduce noise from comparator and ref. voltage
    - Correct code gaps



Simulated INL: PGA+ADC



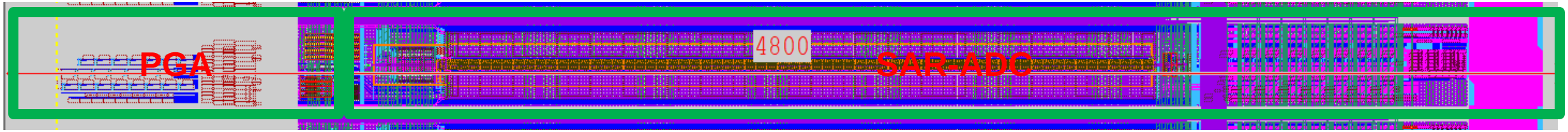
Single ended input with PGA gain: 0dB
INL= 1.8 LSB



Differential input with PGA gain: 0dB
INL= 1.34 LSB

Video channel summary

Spec	value
Sampling frequency	100ksps
Input swing	PGA (0dB): 0~3.3V
Input R & C	R>2Mohm, C<5pF
Resolution	16 bit
DNL, INL	INL, DNL < 1.5 LSB
# of ADCs	32+4+2
Total current	<2mA per ADC channel
Power off feature	Each ADC separately enabled
Input mode	Single-ended, differential, chopping Programmable input current
Sampling mode	Both time interleaving and parallel sampling
ADC clock	3.2 MHz
Noise	<1 LSB



Others

- ROIC Control I/Os :
  - LVDS, single-ended programmable
  - Programmable Logic level
    - 2 for 32 single ended output (1 for 16 output)
    - 1 for digital input
    - 1 for SPI interface
- Fully programmable sequencer
- 4 wire bus for internal electrical property monitor
  - I/V measurement: LDO,V dec, on chip T sensor….
  - Video channel auto test…

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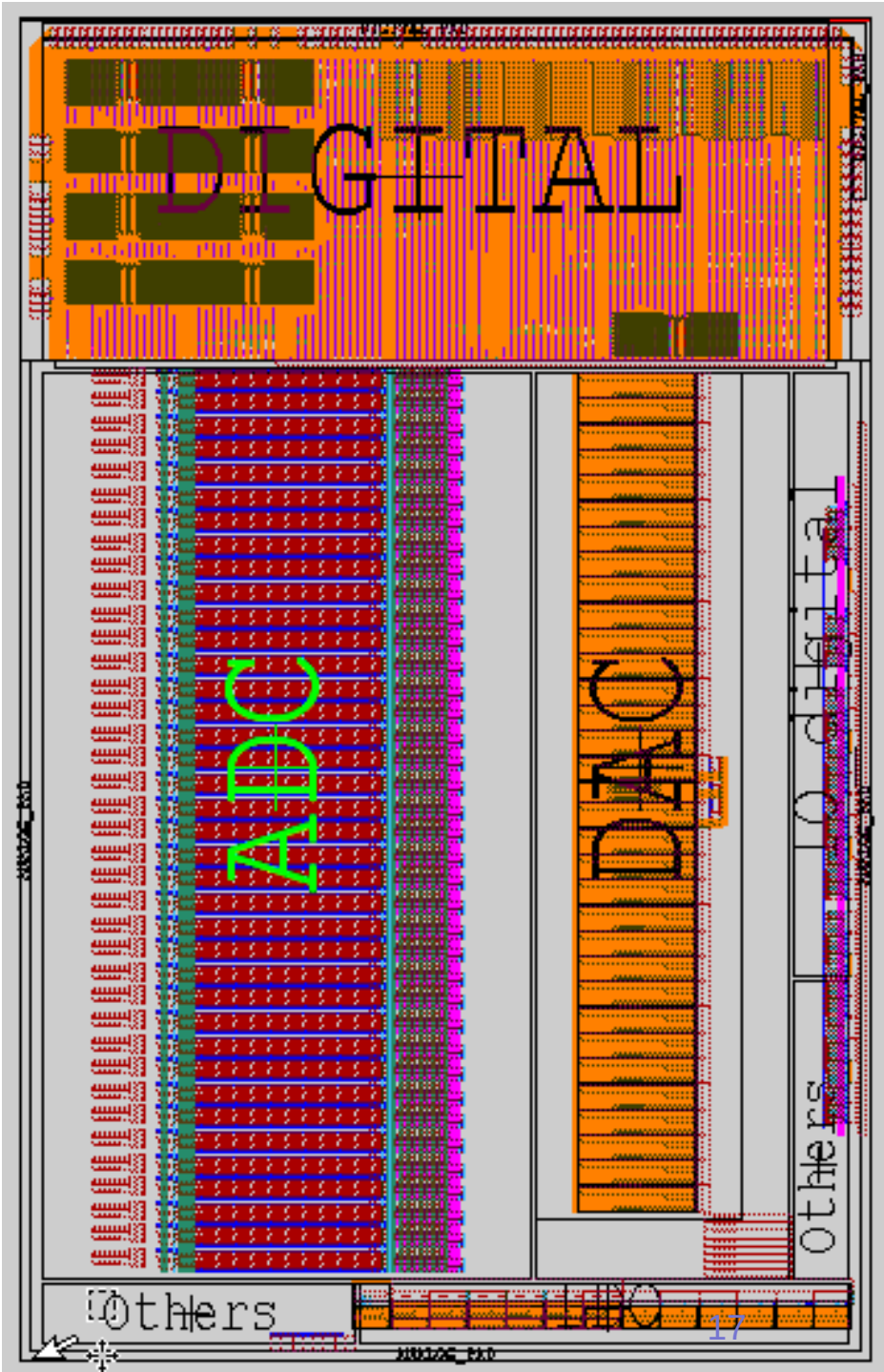
Take home message

- All features to drive and interface IR FPAs
- 36 channel 16-bit analog data acquisition
- Fully programmable sequencer
- Biasing, IO control, housekeeping
- Radiation hard
- Cryogenic: target at 35K (Q3 2020 at SRON)
- Tapeout Q1 2020



Thank you!