A Phase locked loop or frequency multiplier for image sensors

We invite smart and creative students to do their internship and master thesis at Caeleste, working in one of the image sensor design teams.

Image sensors are amongst the largest mixed signals devices. They run on a number of supply voltages and on a number of clocks, with widely different frequencies and phases, between a few kHz and GHz for the LVDS or CML communications. In order to limit the number of IO paths, one typically derives all or most of these clocks from a single master clock. Such happens in a phase locked loop (PLL) block in the periphery of the sensor.

A major issue with this approach is that the high frequency clocks are distributed from a central point. This creates several design bottlenecks related to crosstalk, synchronous clock trees, temperature gradients, hot spots, phase noise and stability. Also individual tuning of phase shifts is not obvious.
We want to explore the alternative to design distributed multiple, smaller, single frequency PLLs or frequency multipliers, resulting in an overall more compact, less power hungry and still faster system.

The works will include

- Conceptual study and comparison of PLL and frequency multiplier architectures
- Studying the inclusion in a few target image sensors, with the larger team
- Schematic IC design and simulation
- Layout design and post-layout verification
- Contribution to the overall image sensor design
- If in schedule, participation in the characterization

The thesis work includes a prior internship; the total duration of the thesis exceeds 6 man months.

For further information or applications contact jobs@caeleste.be.