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Photon imaging with monolithic CMOS SPADs

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Purpose

Why a 2D array of monolithic SPADs?

Mainly for applications requiring precise information of the time of arrival of the photon. e.g.

- Photon counting
- Coincidence detection
- Time Of Flight imaging, distance ranging, approach, docking
- Fluorescence decay
- Spectroscopy
- X-ray, gamma, HE particle detection

Purpose

Our specific goal

- to explore tunability of performance parameters
 - QE(Quantum Efficiency)
 - DCR(Dark Count Rate)
 - After pulsing time
 - In std 0.18 μ m technology

Outline

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- **Introduction: The SPAD principle**
- **Layout of SPAD and SPAD arrays**
- **Measurement results**
- **Conclusions**

Outline

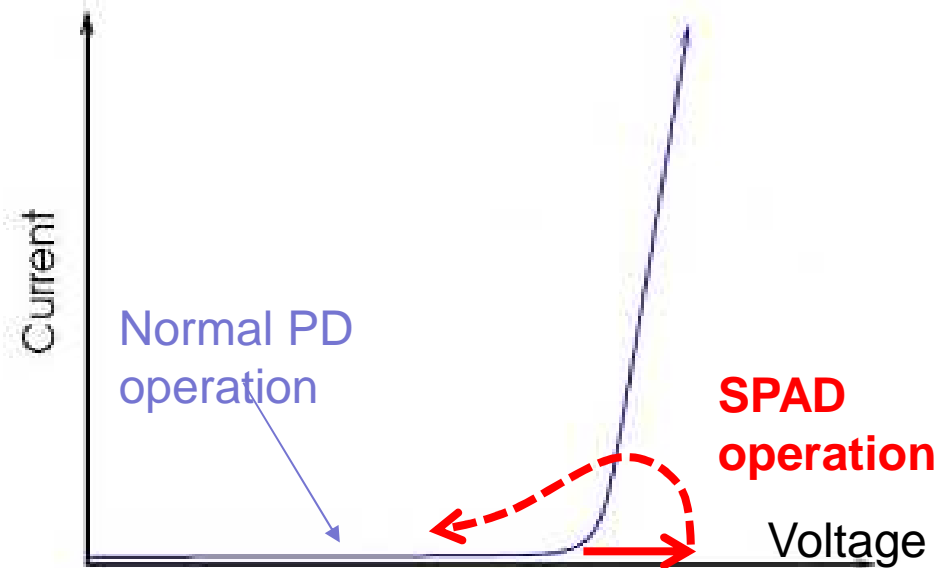
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- **Introduction: The SPAD principle**
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The SPAD principle

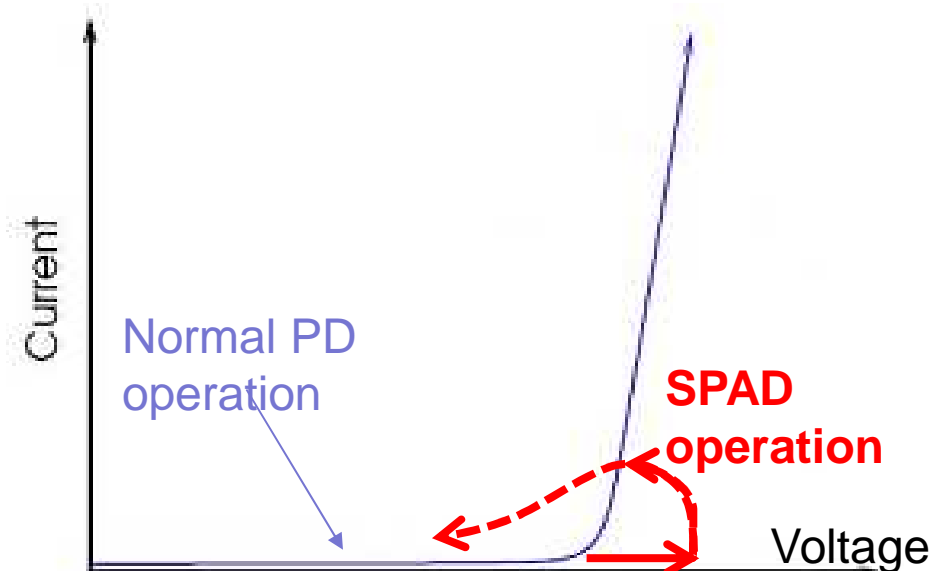
SPAD or “Geiger-Mode” APD

- Operating point beyond breakdown voltage



SPAD background

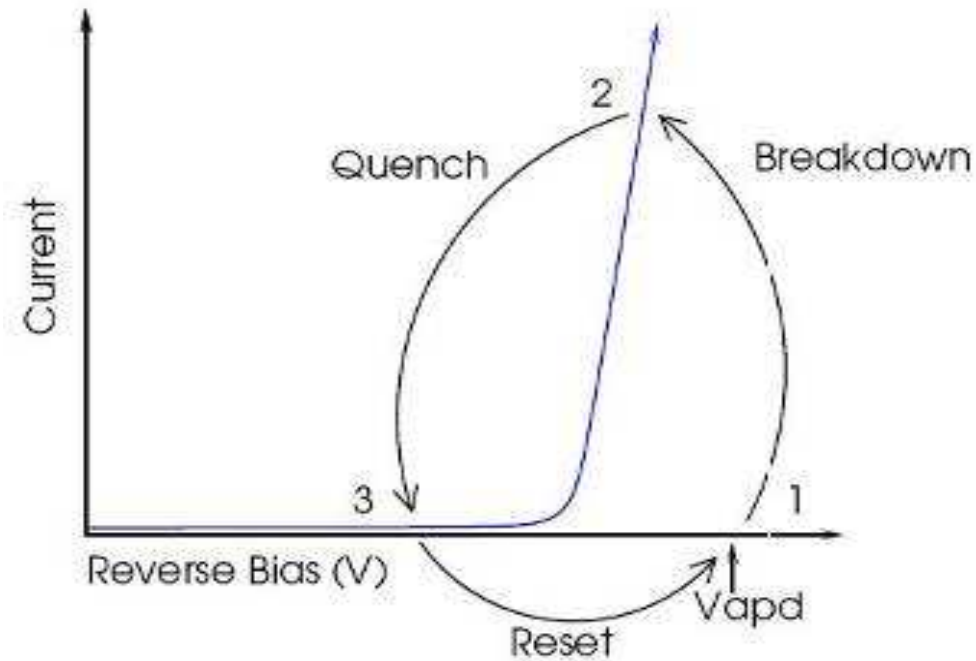
- Recharge (Reset):
 - Voltage beyond the breakdown value is applied and stays there until...
- Sense:
 - An electron (due to photon/dark current) causes breakdown and hence a huge current.
 - The drop in voltage is sensed with appropriate analog circuitry.
- Discharge (Quench)
 - Residual charges are drained out completely.



SPAD background

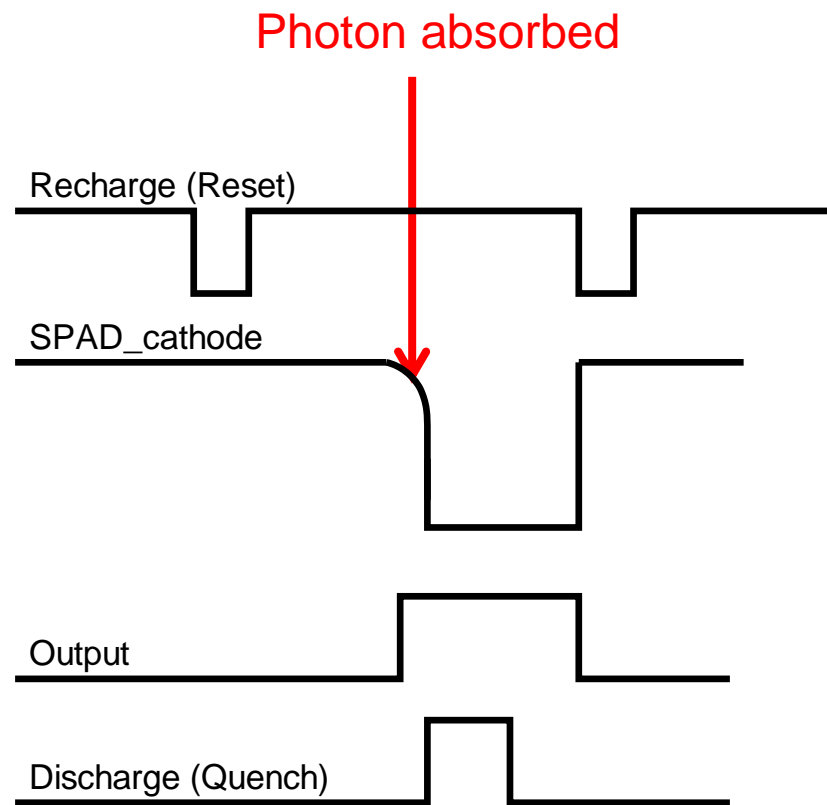
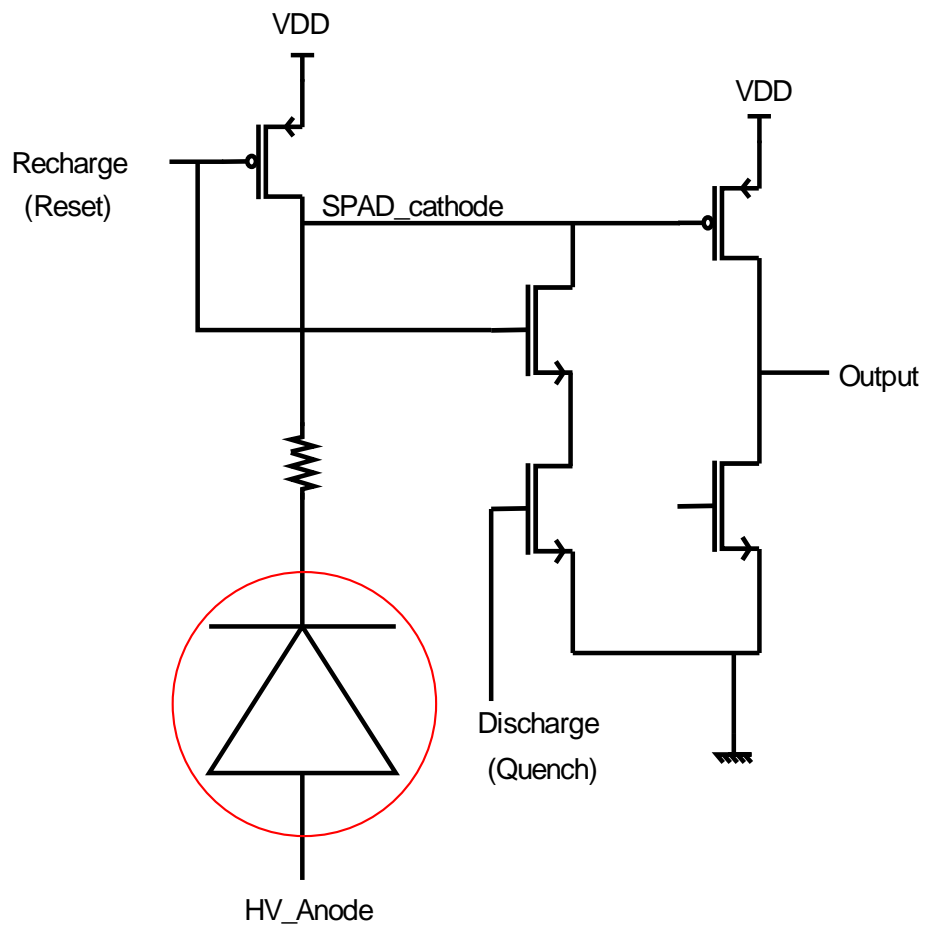
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Summary



SPAD circuitry

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SPAD LAYOUT

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➤ **SPAD topologies**

- How to use available layers in the CMOS process to create SPADs and their guard rings

➤ **SPAD array**

- Create a complete 32x32 SPAD pixel image sensor

➤ **SPAD pixel layout**

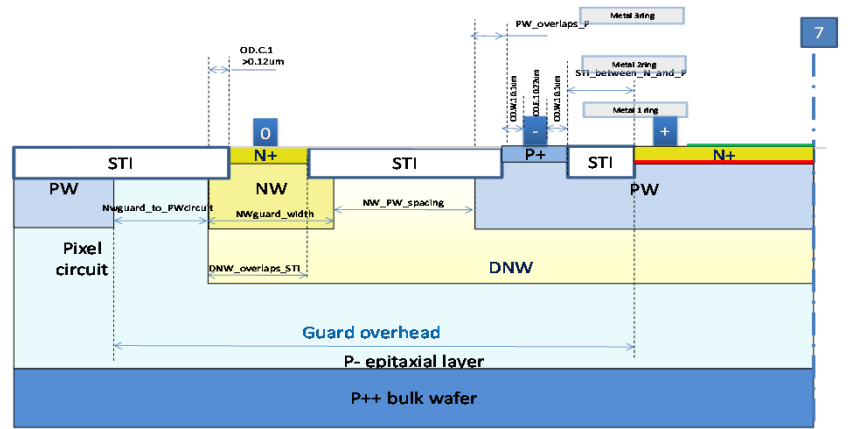
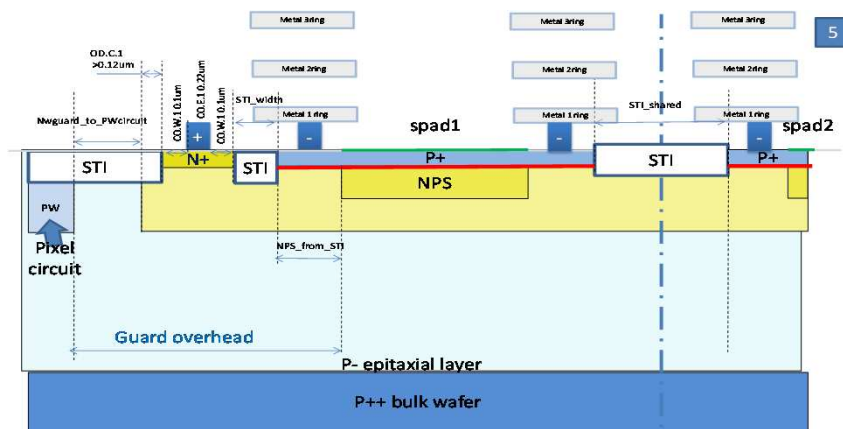
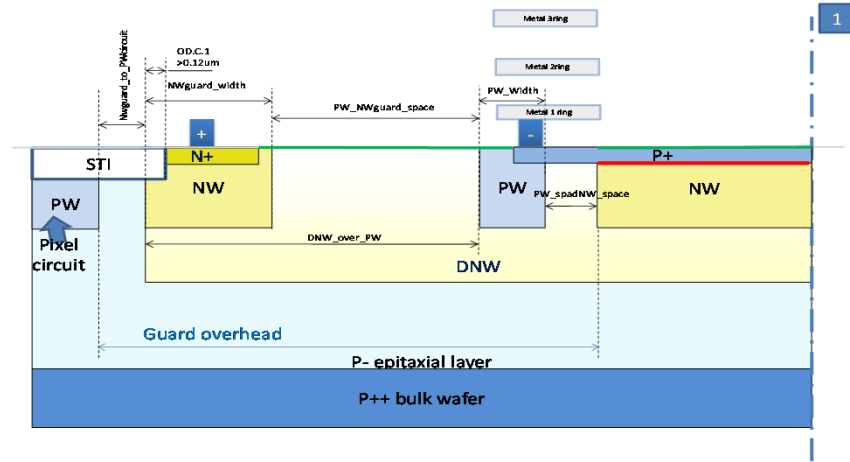
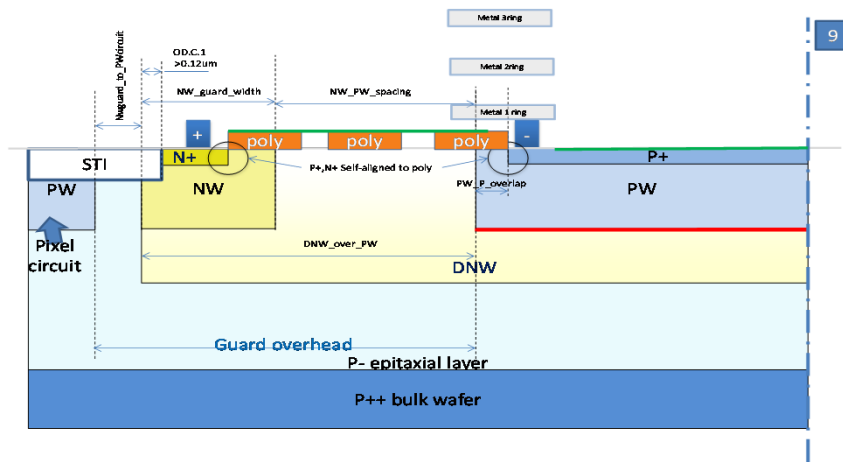
- Geometry, spacing, combination with in-pixel logic

➤ **SPAD variants**

- 7 different topologies, 5 different guarding types, sharing or not sharing guards, cathode or anode readout, dimensions
- In total 120 variants

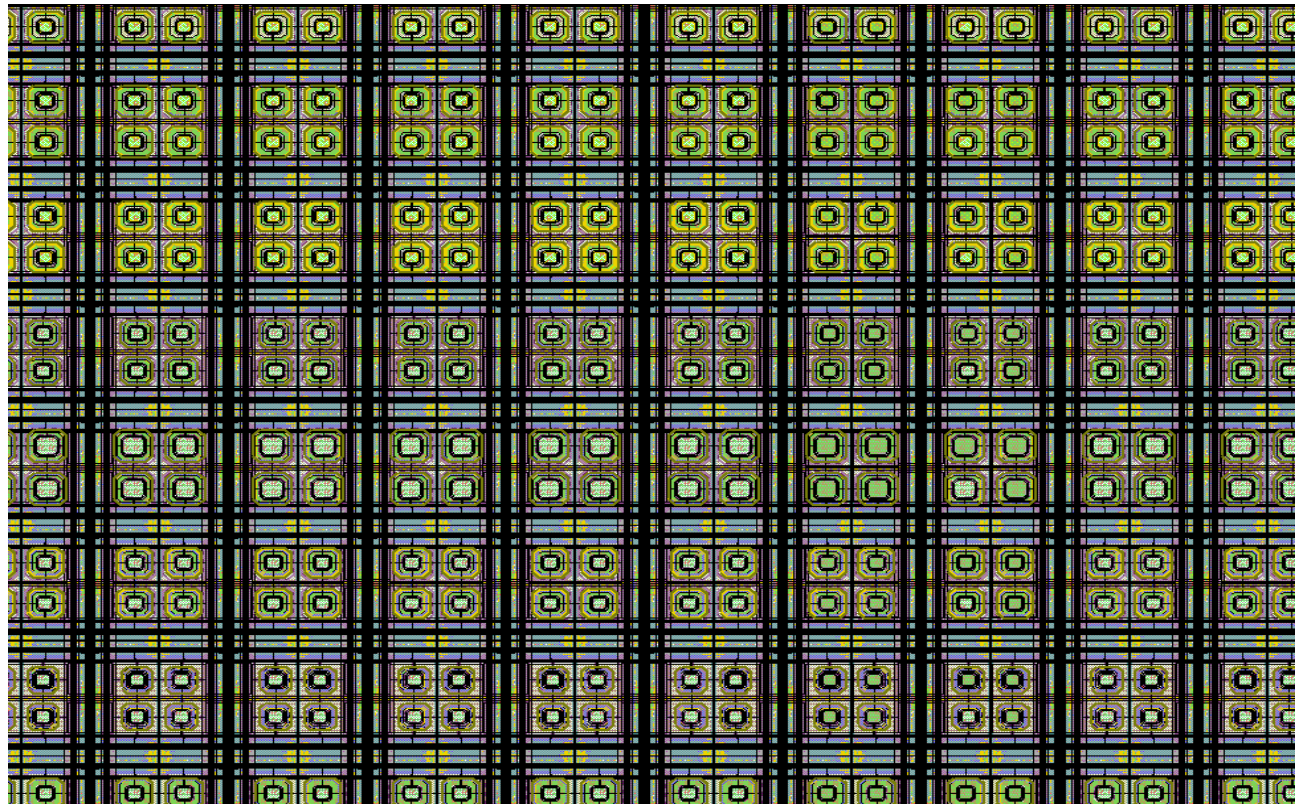
SPAD topologies

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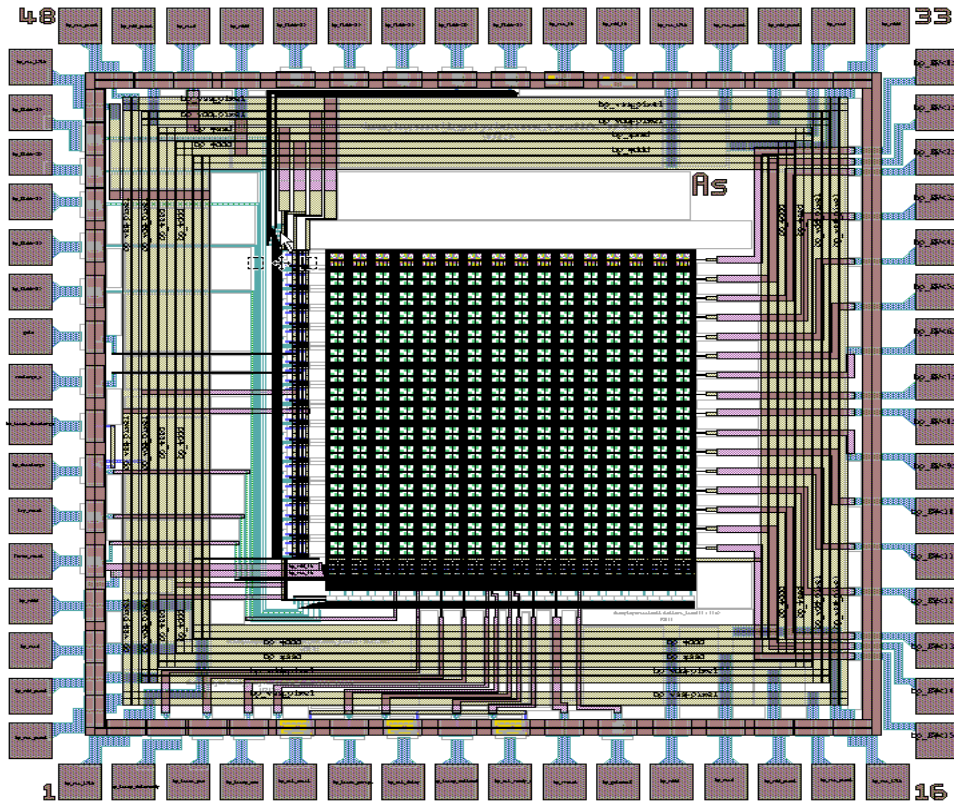


SPAD array

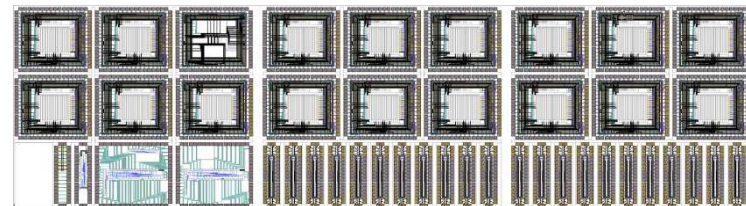
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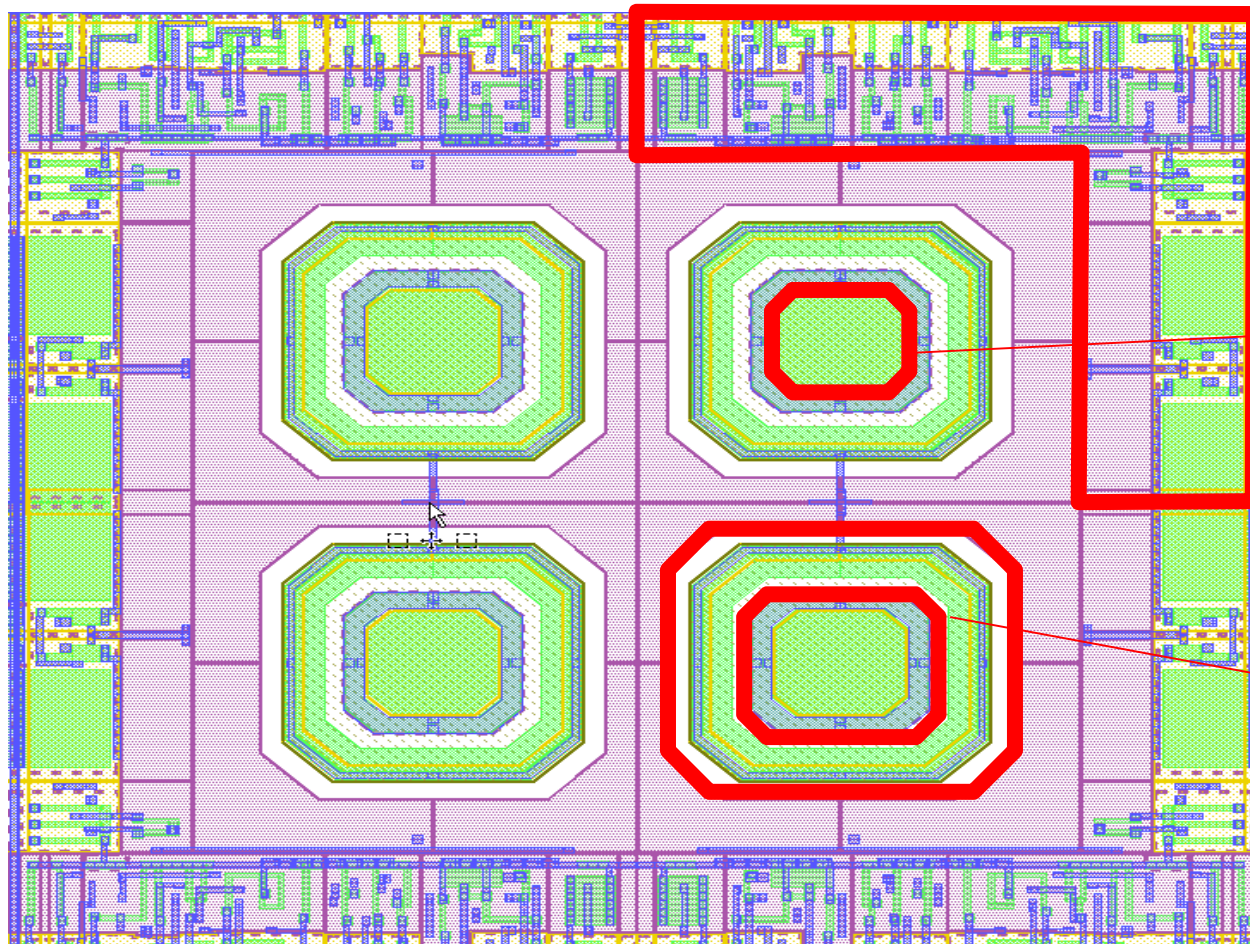
SPAD array prototype caeleste



- 32x32 pixels
- 16 types (variants) per such array (frame) organized per 2 rows.
- Each 2 rows of SPADs can be independently biased
- In-pixel circuitry: reset, quench, analog domain counter, analog output, application specific operators.
- 17 such arrays (“frames”) are designed with different variants pixels



SPAD 2x2 pixel layout caeleste



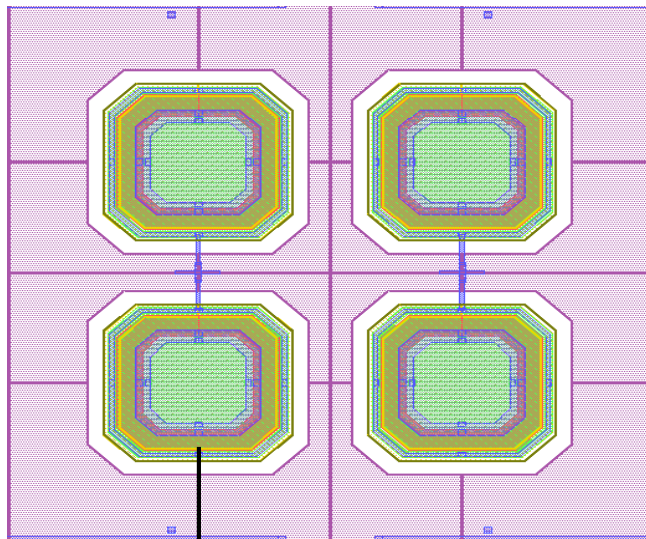
Pixel electronics
(analog domain counter)

→ **SPAD useful area**

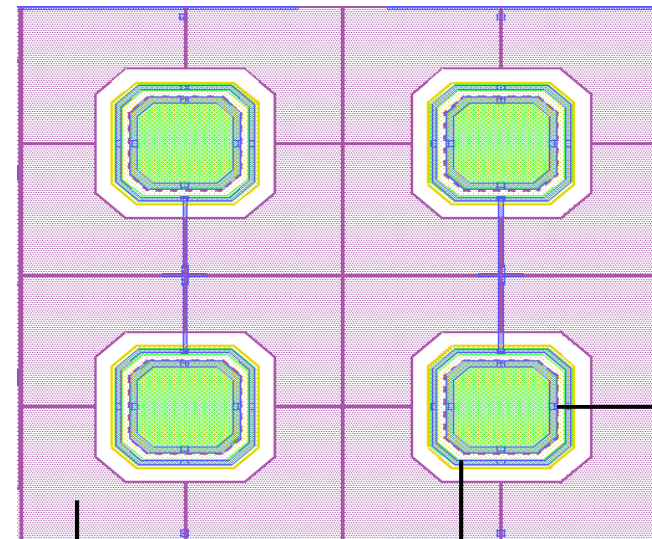
→ **Guard**
(Not common)

Layout Variants

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Guard ring overlaid with poly



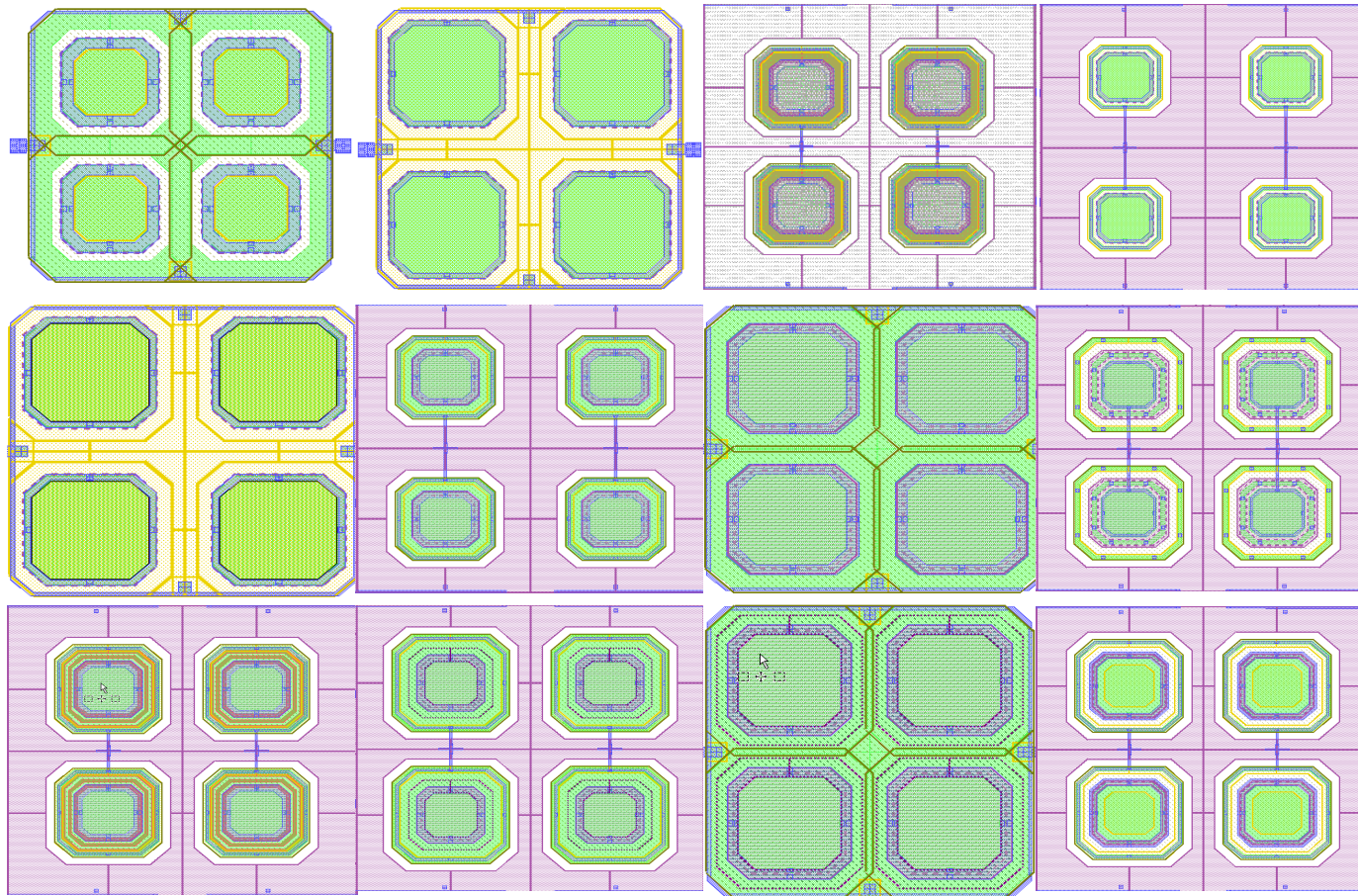
PWell
Substrate

Deep NWell contact

SPAD
Anode
contact

Other SPAD Variants

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Outline

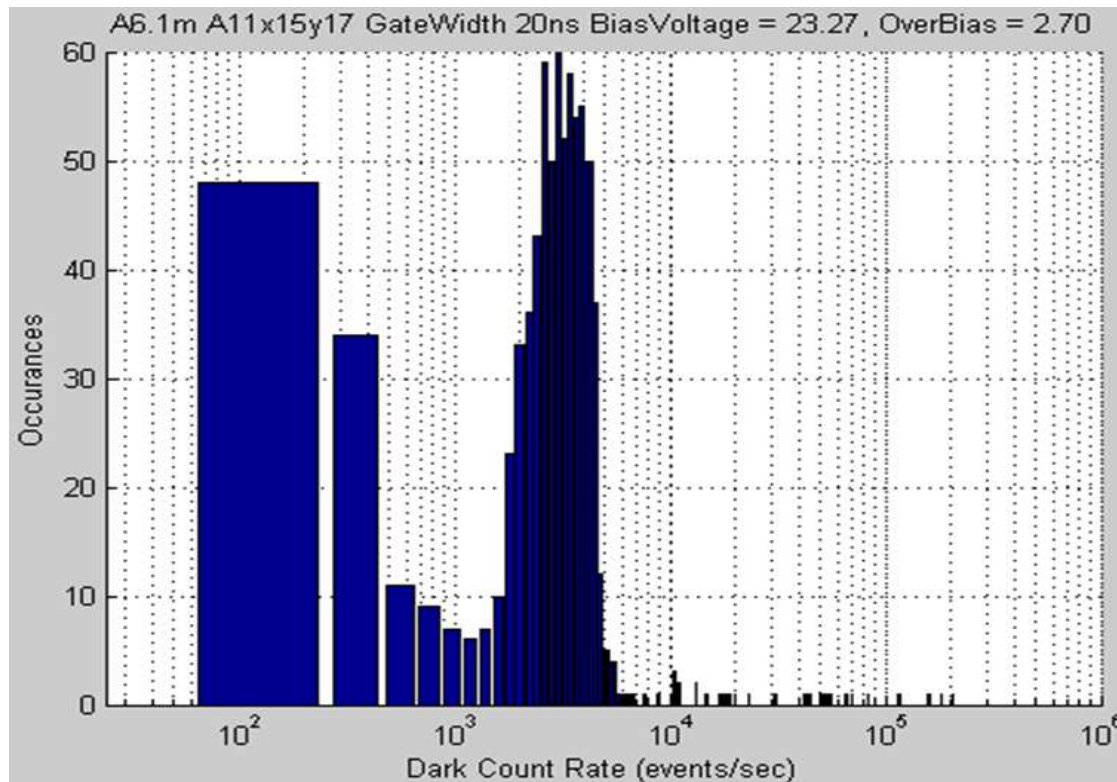
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Measurement results

Dark Count Rate (DCR)

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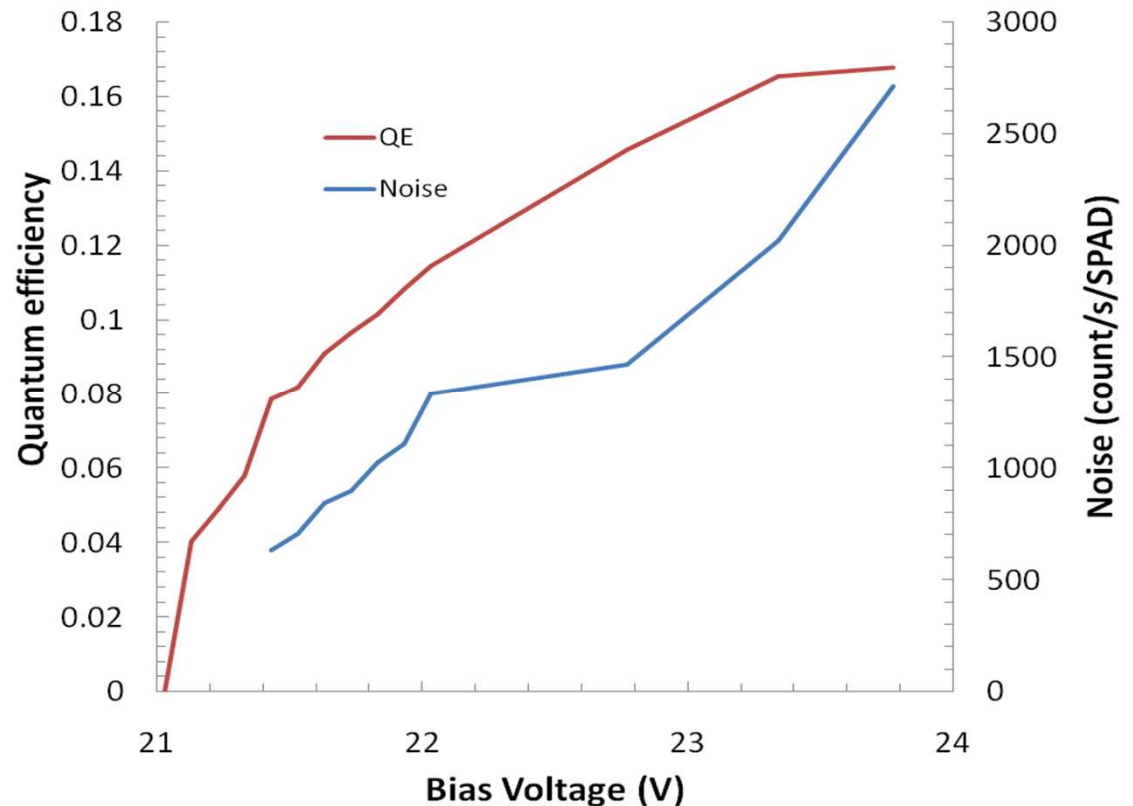


QE measurement I:

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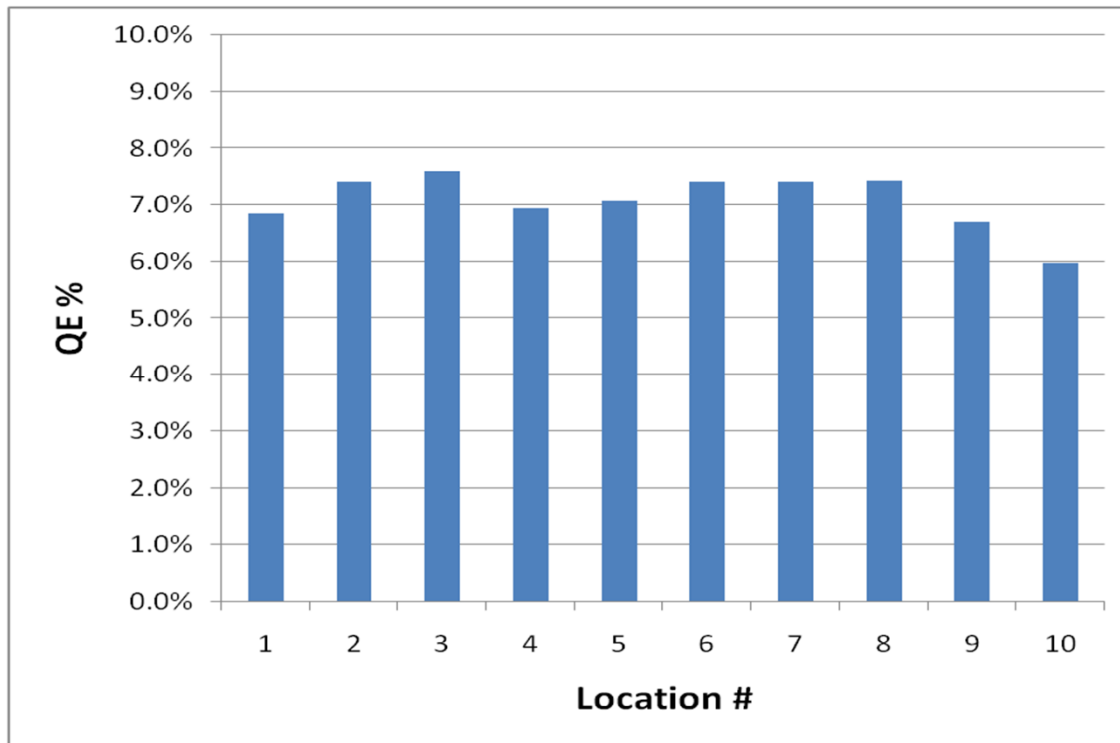
Cathode connected SPAD

- **Threshold voltage: 21.1 V**
- **Over bias up to 2.74 V in the measurement**
- **Max QE is >16%**
- **Noise = dark count rate**
- **660 nm laser**



QE at different locations **caeleste**

10 same pixels in the frame



QE mean = 6.7%
QE STDEV = 0.49%

The variation is quite low:
STDEV/mean = 6.8%

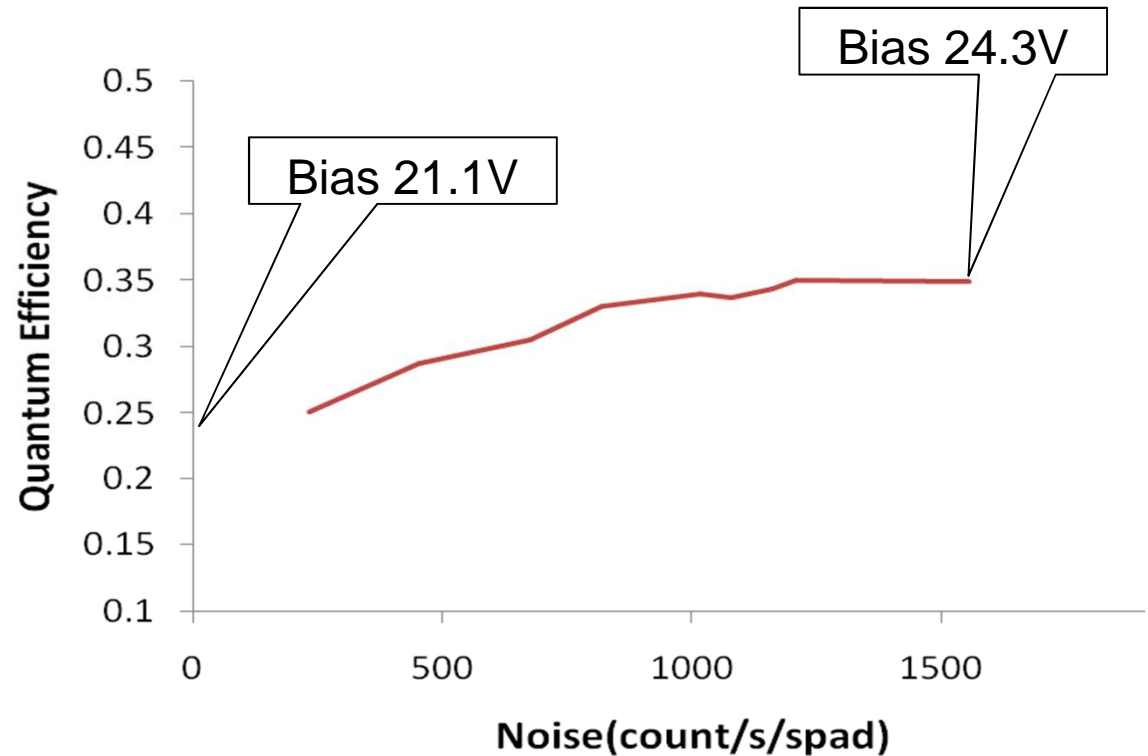
Bias Voltage 21.43 V
(Threshold voltage 21.1 V)

QE measurement II:

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Anode connected deep-junction SPAD

- **Threshold voltage: 21.1 V**
- **Over bias up to 3.2 V in the measurement**
- **Max QE is 34.9%**
- **Noise = dark count rate**
- **660 nm laser**



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conclusions

- **Photon Conversion Efficiency (~QE)**
 - deep junctions, not shallow
 - Deep well, deep and low doped epi layers
- **Within the constraints of the CMOS technology**
 - design rules, available layers and implants
- **It is possible to tune SPADs for a wide range of specifications using a standard CMOS technology**
- **It is found that available layers in the CMOS process can be used far outside their electrical specs.**

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Thank you