caeleste

ICSO 2014
Tenerife

CRYOGENIC AND RADIATION-HARD ASIC FOR INTERFACING LARGE FORMAT NIR/SWIR DETECTOR ARRAYS

SELEX GALILEO
A Finmeccanica Company

P.Gao, B.Dupont, B.Dierickx, E.Mueller,
G.Verbruggen, S.Gielis, R.Valvekens,

esa

easics

About us

- **Image sensors and periphery ASICs**
- **Founded 2006**
- **Mechelen, Belgium**
- **17 p (10 designers)**

Supplier of Custom designed
Beyond "State of the Art" CMOS Image sensors and ASIC for
Space, Scientific, Industrial and **Medical** applications

Outline

- **Motivation**
- **Architecture and building block design**
- **Design for Radiation hardness and Cryogenic temperature**
- **Test results**
- **Conclusions & future work**

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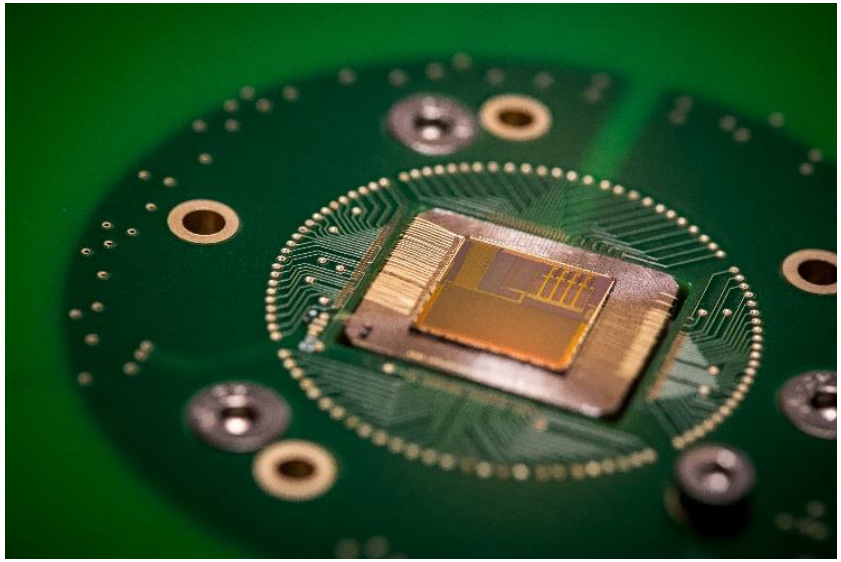
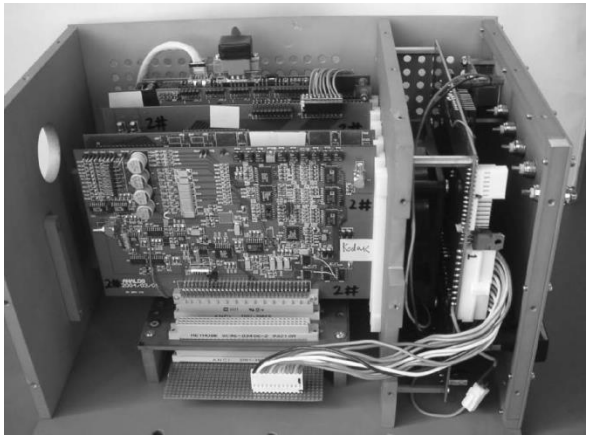
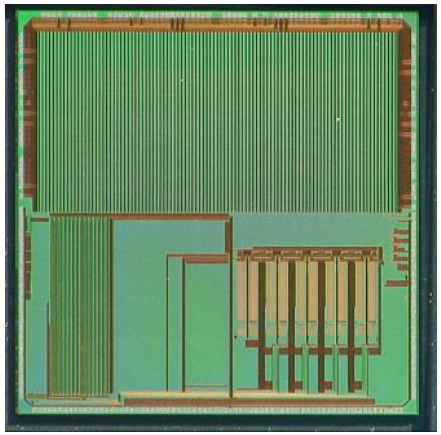


Why an ASIC ?

To operate an IR imagers



[Z.Zhao.SDA'05]



Analog domain

- Signal conditioning
- Analog to digital converter
- Regulated power supply
- Bias voltage/current references

Digital domain

- Digital control core
- Memory & Clock
- Data Communication

The ASIC

This development aims at providing the community with a IR imager accompany ASIC

- **Tailored to imagers (especially IR sensor)**
  - Easy to control
  - Simple to intergrade
- **Taking in consideration multiple IR detector manufacturers specificities**
- **Wide operating temperature range (77k – room T)**
- **Able to drive multi-sensor/array systems**
- **Radiation hard**
  - 1Mrad TID
  - 60MeVcm^2 /mg SEU

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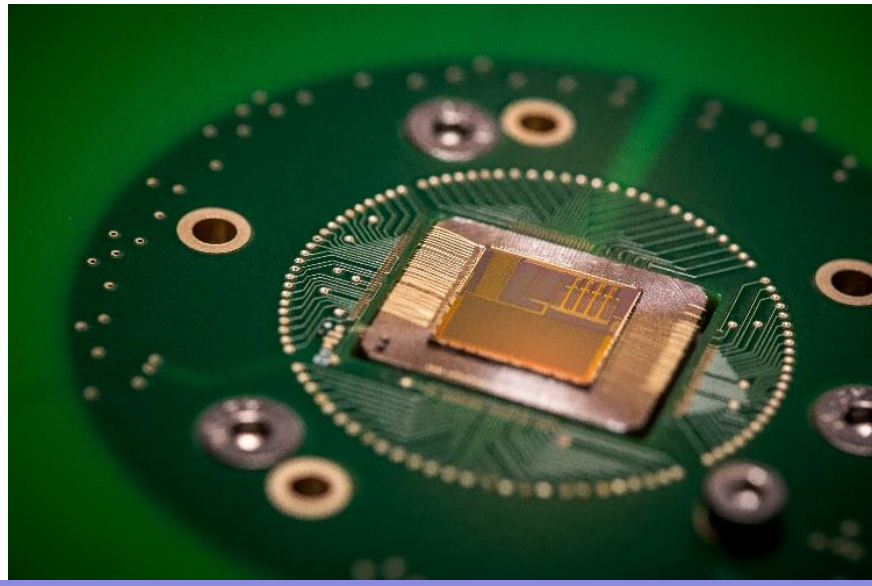
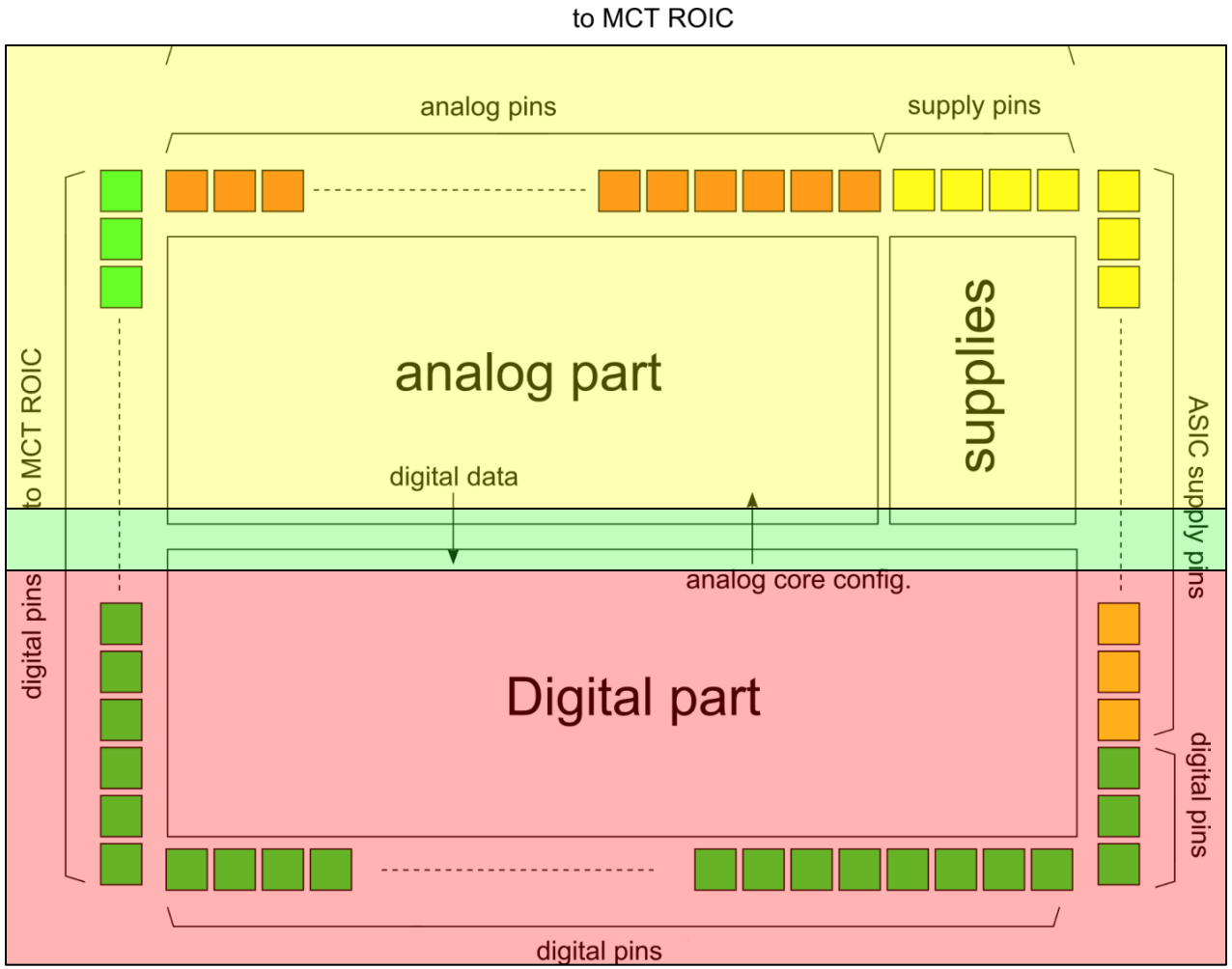
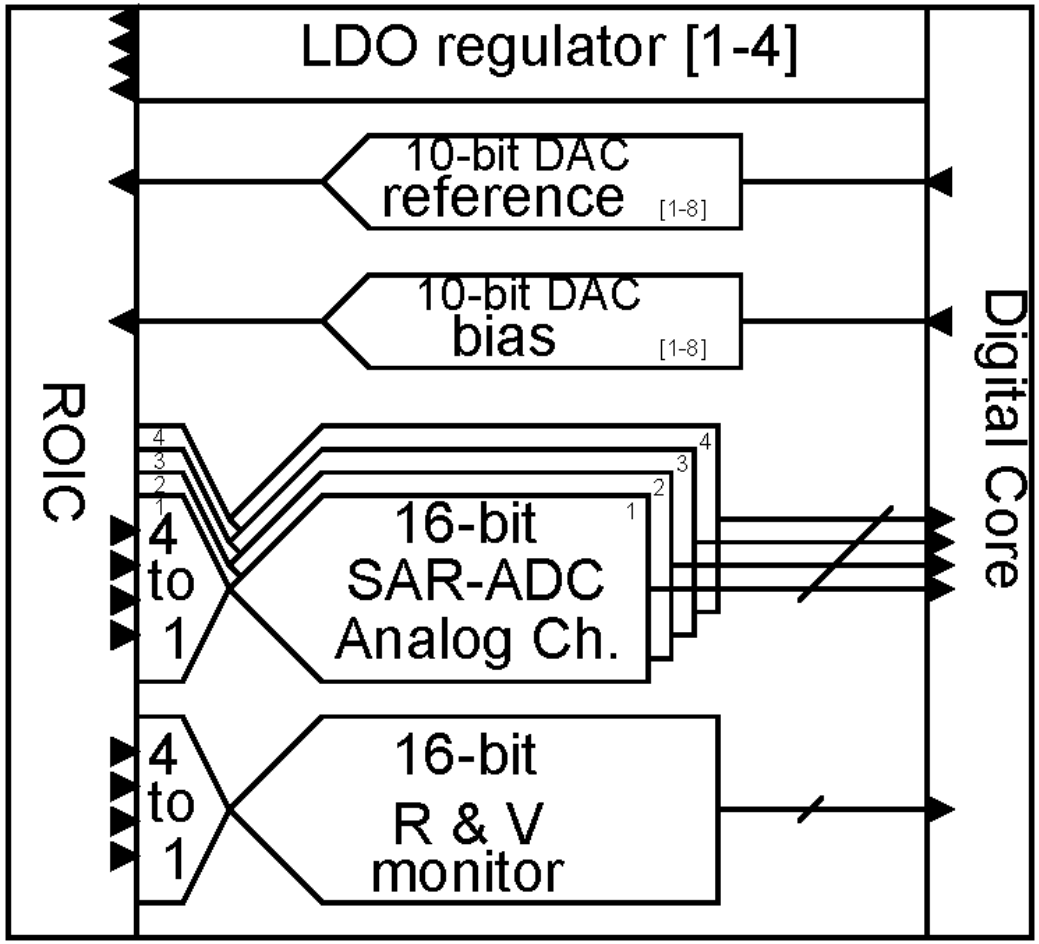


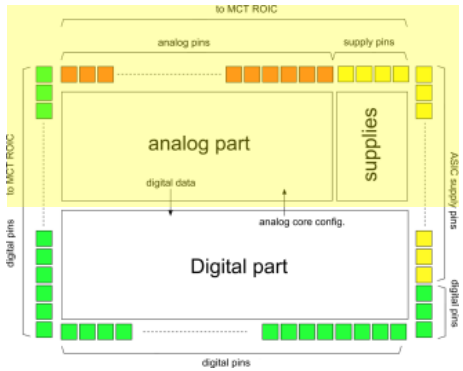
Architecture

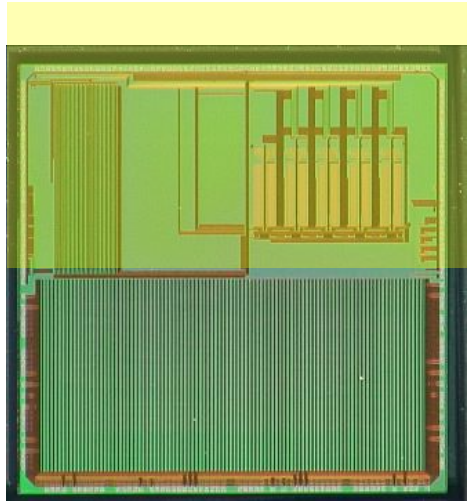


Analog section



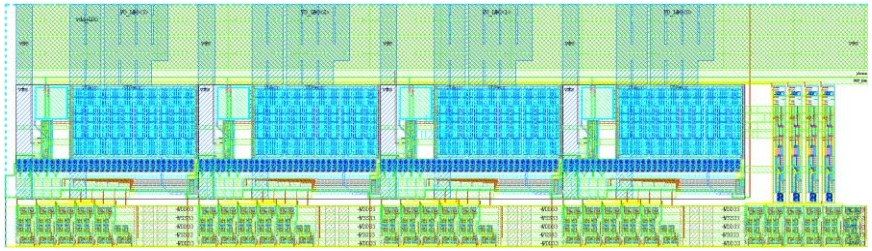
Bandgap
T sensor



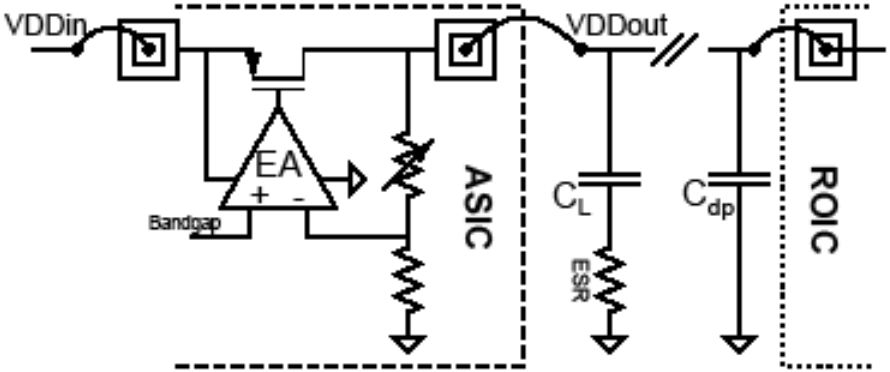


Supply

- LDO
  - Programmable output
    - 1,3…3.4V
  - Stability: PM>60°
  - Output current 0-100mA

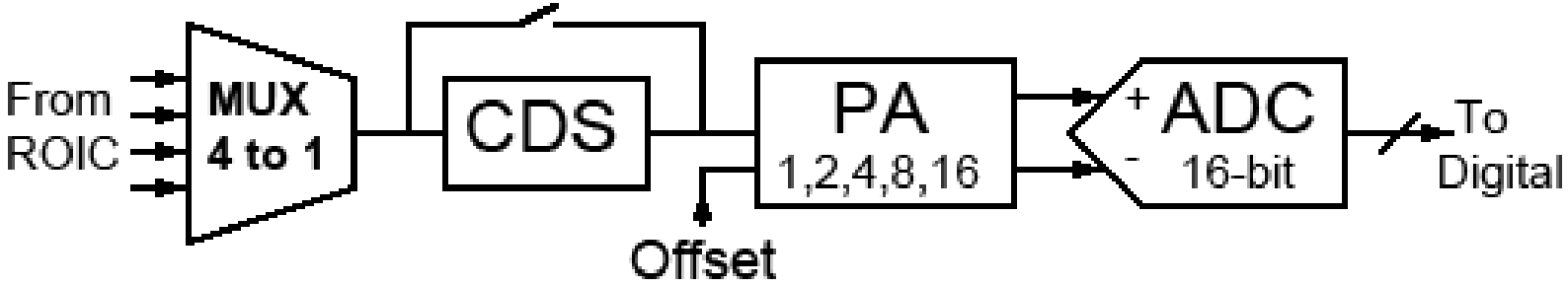


- Bandgap
  - 1.2V
  - 77K-300K



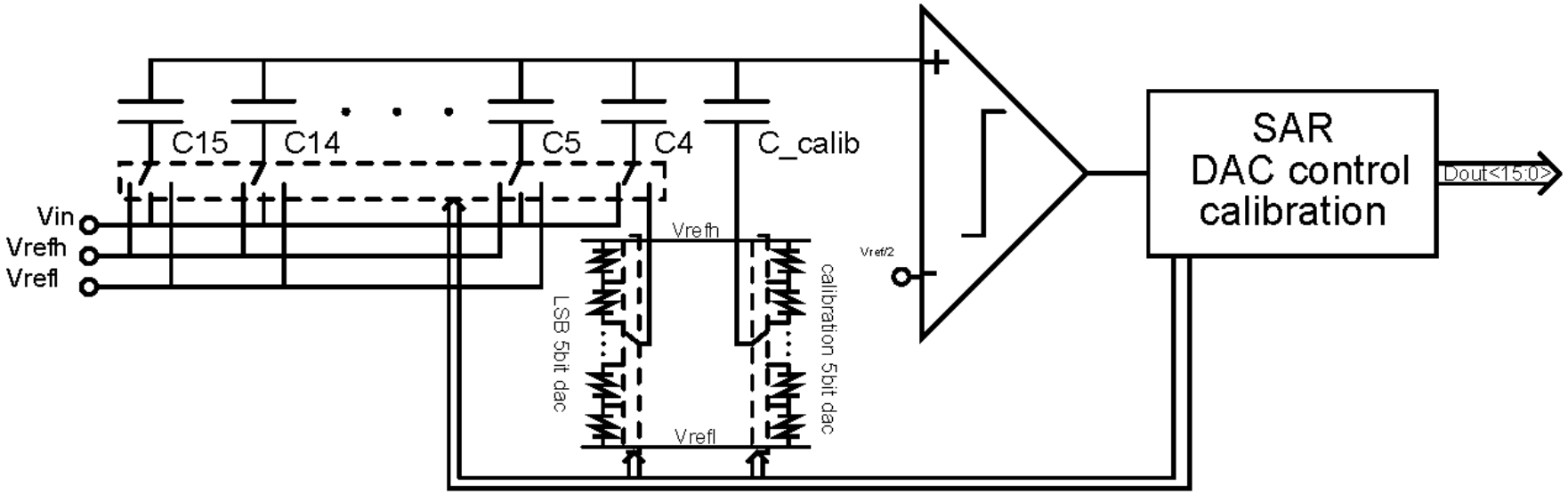
Conversion channel

- One ADC addressed 4 analog inputs in prototype ASIC
- CDS
  - Bypassable
- Preamplifier (PA)
  - Programmable gain from 0-30dB in 6dB step
  - Offset cancellation (8-bit)
  - Single to differential

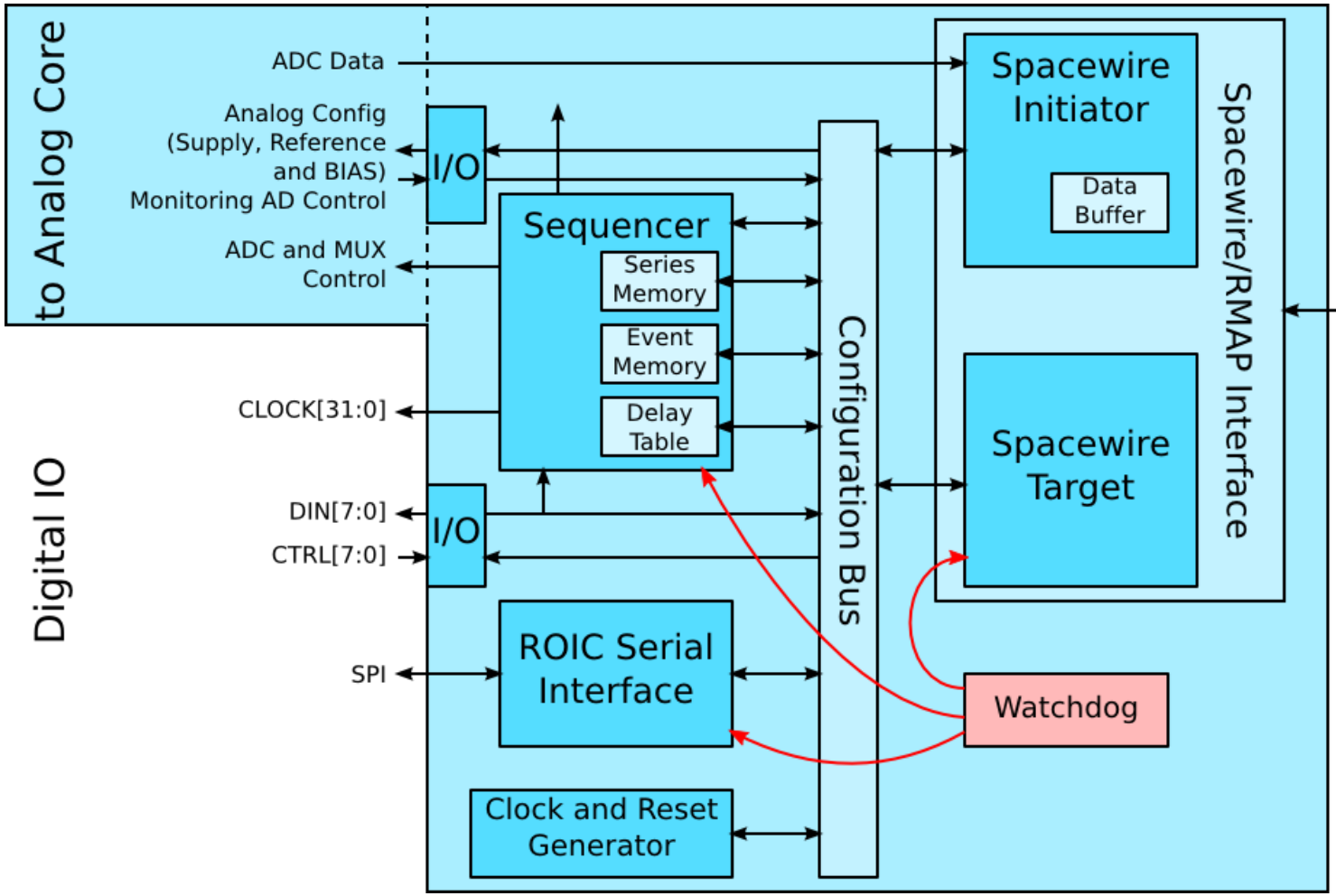


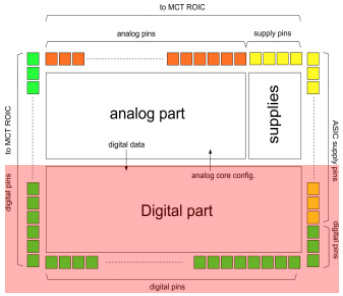
ADC

- 16-bit, 100kHz, fully differential SAR ADC
  - Hybrid feedback DAC
  - Low offset comparator auto zero
- A calibration scheme is implemented



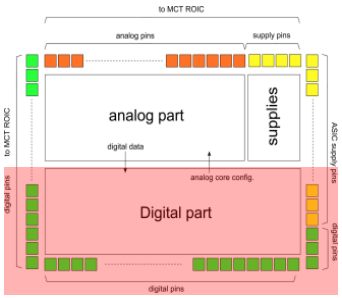
Digital section





Specifications

Digital domain	
Master clock	0 – 200 MHz
System level protocol	2 – 200 Mbit/s Space Wire
ROIC digital control	32
ROIC monitoring and trigger inputs	8
Scheduler time granularity	10M updates/s
Sequence nesting depth	8
ROIC programming channel	1 SPI



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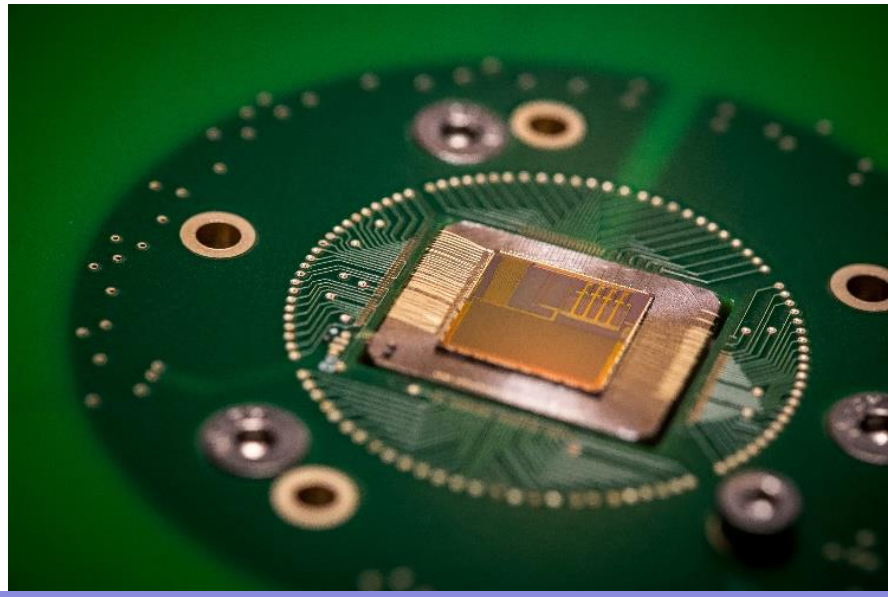


Radiation hardness: digital

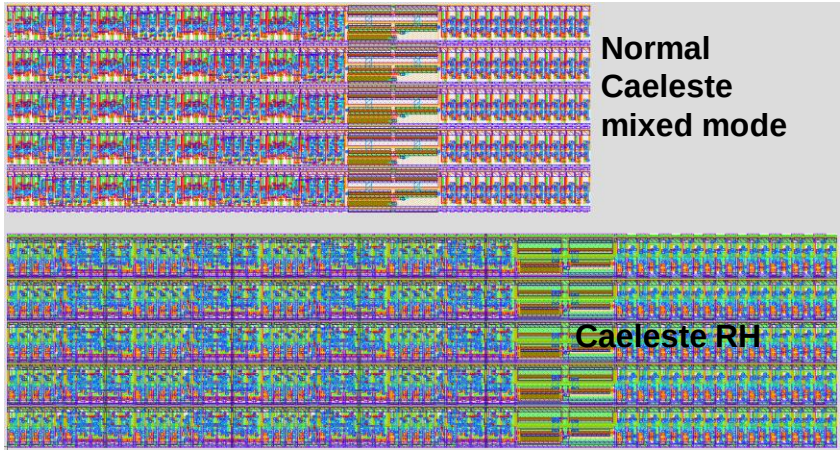
- Synthetized digital logic
  - DARE lib (IMEC & ESA)
    - 0.18 um CMOS 1P6M
    - Digital cell with TID, SEU, SEL tolerance
    - Allows custom mixed-signal design
  - Redundancy
    - Hamming Codes
    - Parity check
    - Safe FSMs
  - Watchdog Timers

Radiation hardness: analog

DARE has a limited subset of analog component.

Caeleste developed its own radhard cells

- Analog and High Voltage logic standard cells
- Full custom tactical cells
  - Analog & mixed mode
  - TID & TnID hardness
  - SEL hardness
  - SEU hardness without TR
  - <20% increased Cin and power
  - <50% area increase



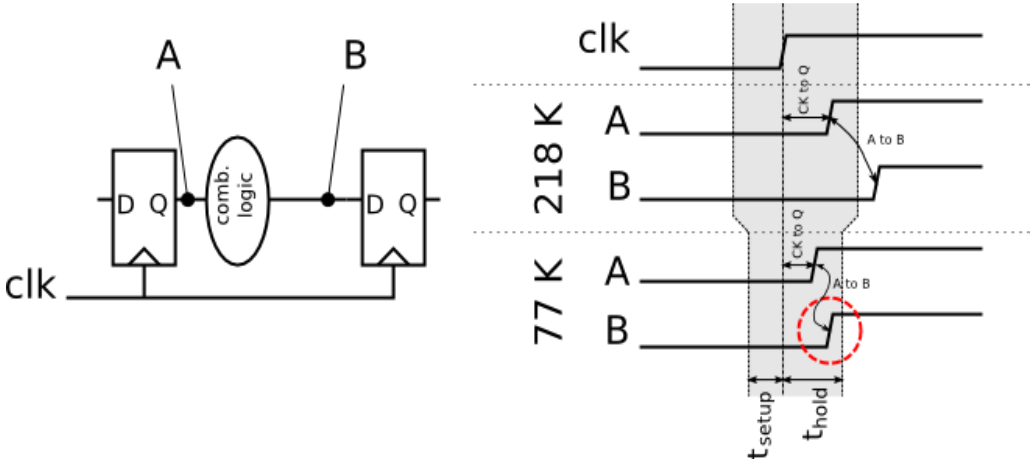
Design for low temperature

- Synthetized digital logic:
  - A derating of speed, power, etc. of the library
  - SRAM
- Analog custom design:
  - Active component modeling
  - Component selection

Cryogenic digital design

The DARE library has never been used at 77K before

- Faster but risk for set-up and hold time violation.

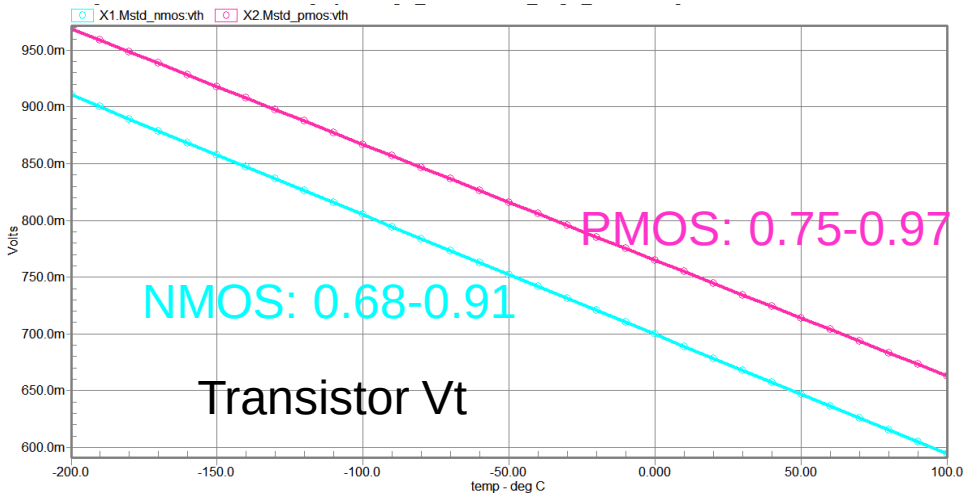


  - Adapted models based on characterization at 218K

- SRAM has not been validated before
  - Backup registers

Cryogenic analog design

- MOSFET modeling
  - V_{th}: increase
  - Mobility: increase
  - MOS switch: low R_{on}



- Passive components
  - Highly doped non silicide poly Resistor for stability
  - MIM capacitors
- Rely on ratios not absolutely values

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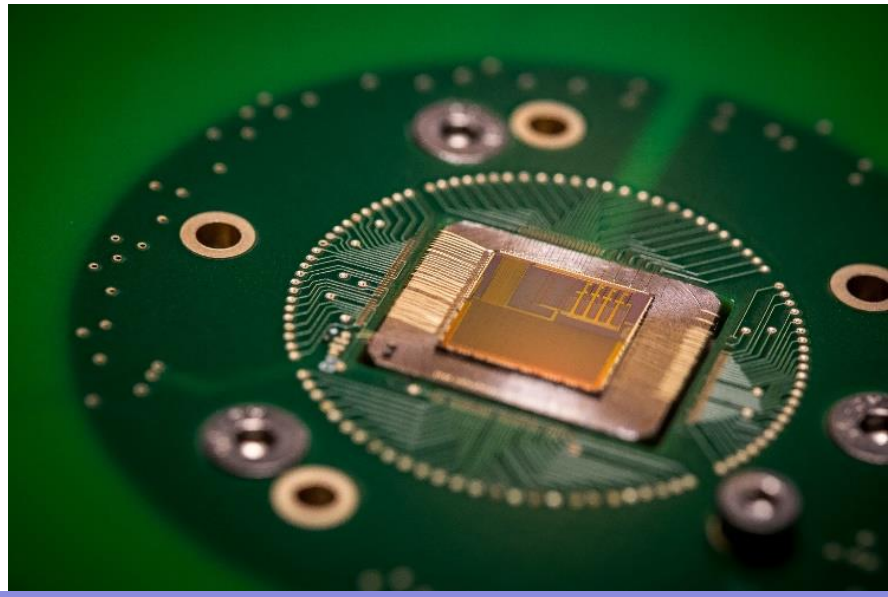
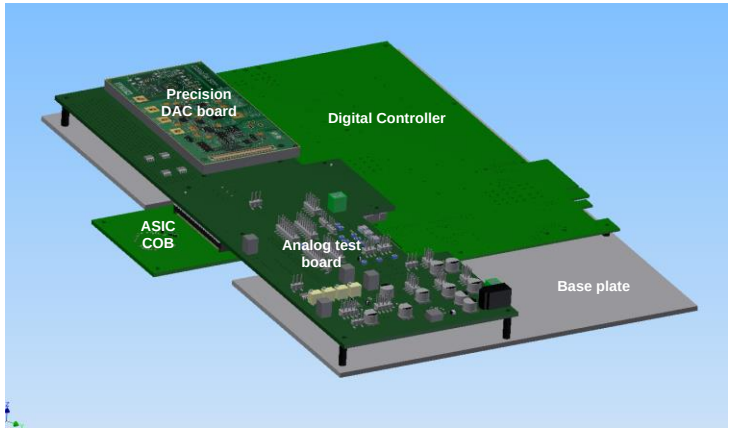


Test setup

Unified design for:
RT board
CT board



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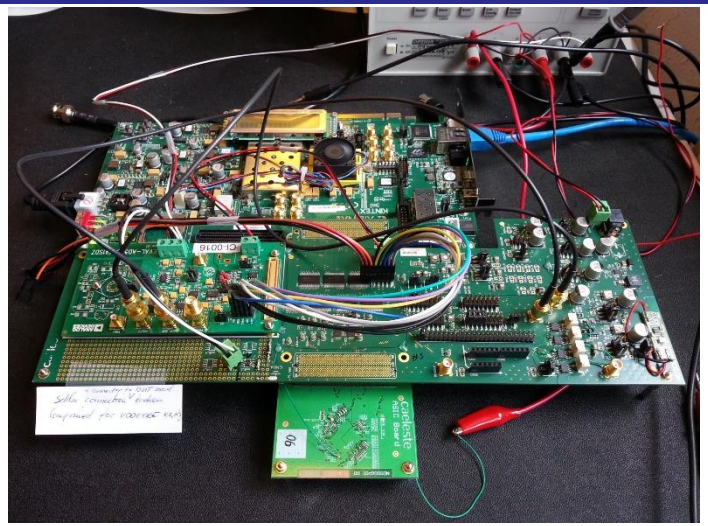
RT board



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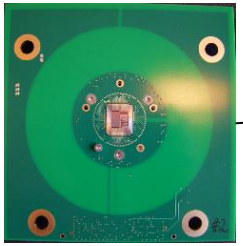
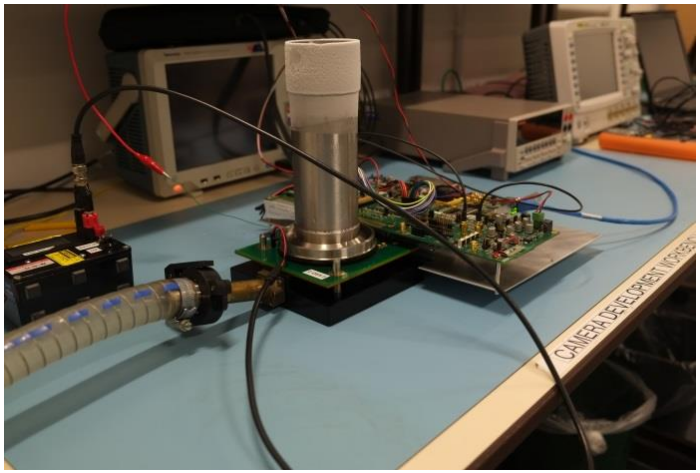
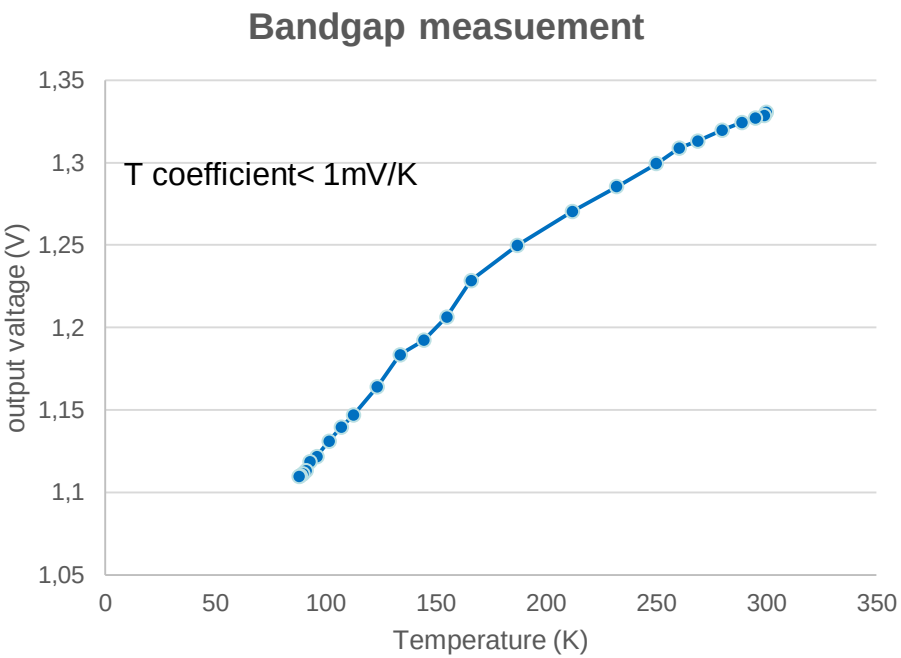
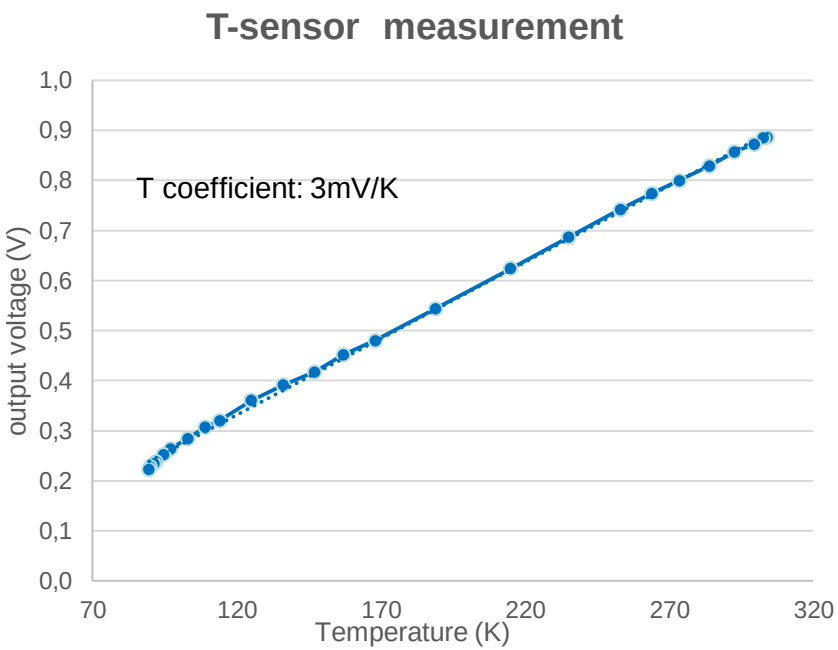


CT board

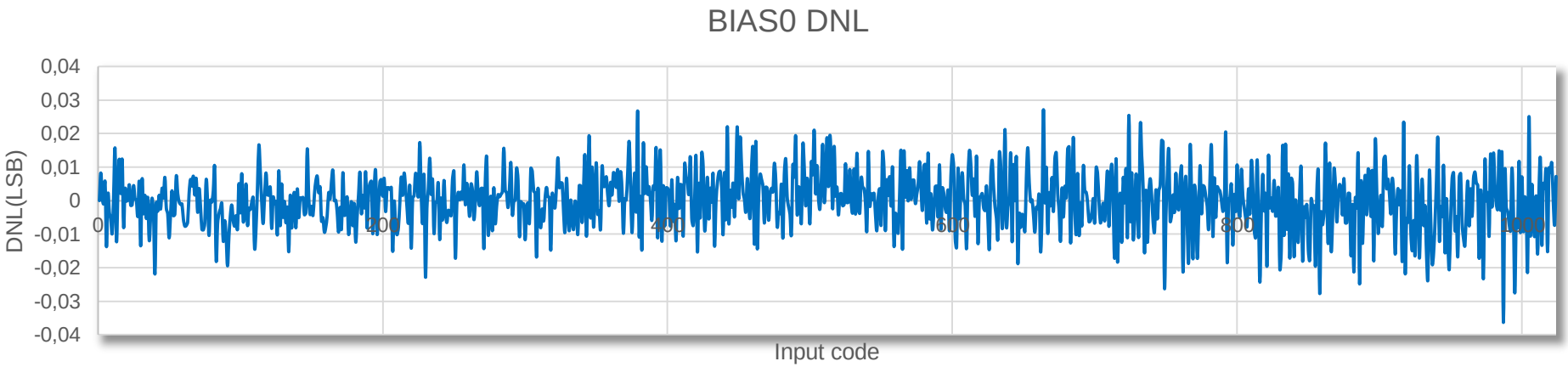


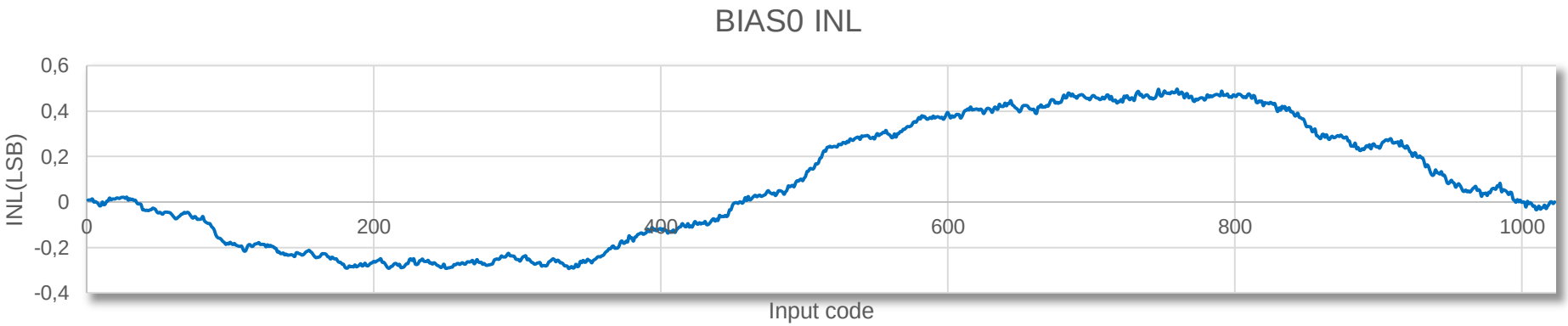
Bandgap and temperature sensor





Reference and Biases 10-bit

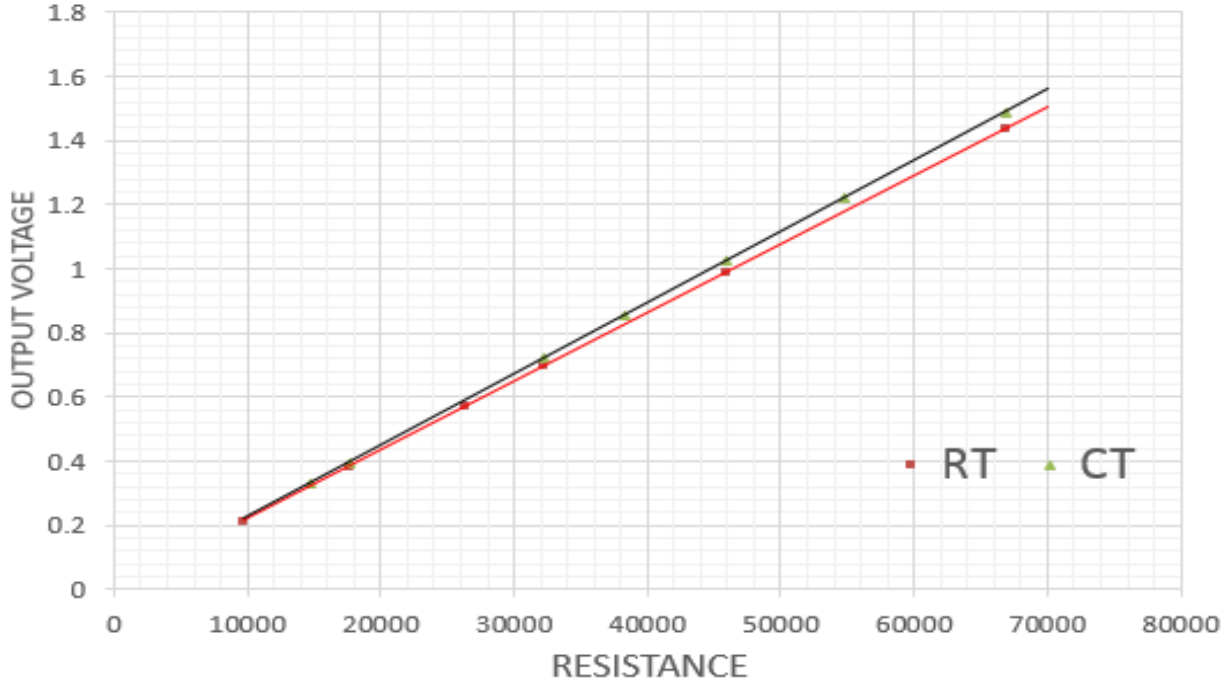




R monitor

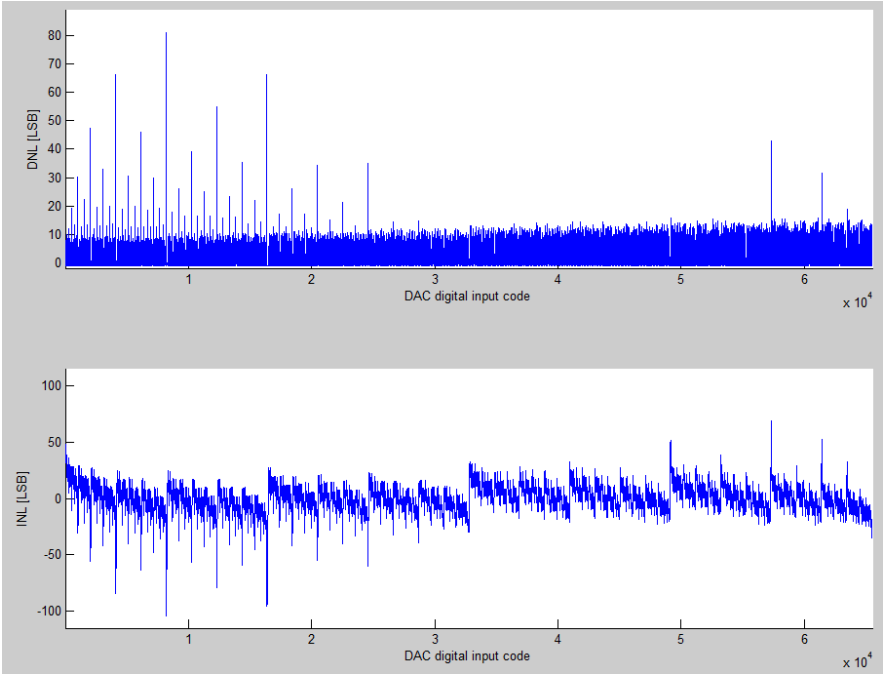
- **On chip SC current source.**
  - R range 10k – 70k ohm

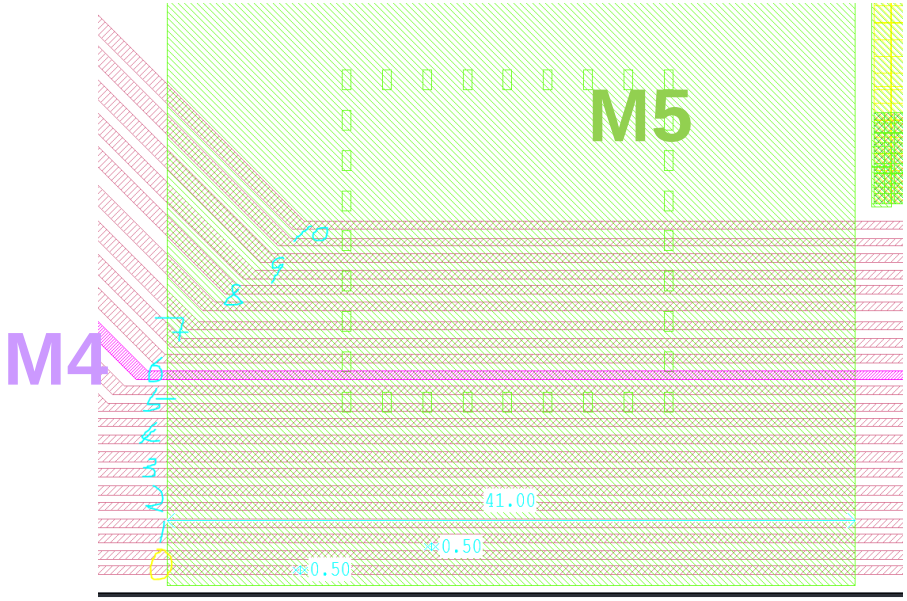
Measured output voltage with 2MHz clock

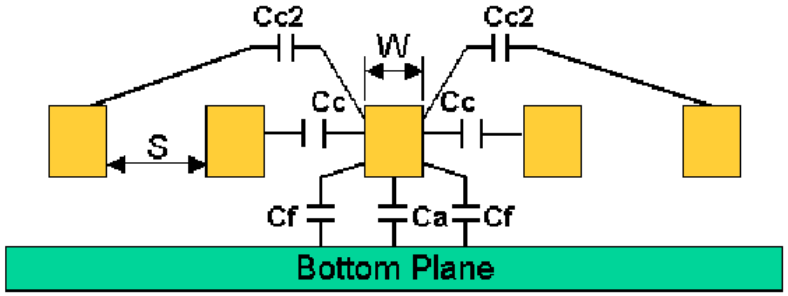


16-bit SAR ADC INL DNL

- **INL DNL problem :**
  - Root cause is a AC coupling in the **layout: 2 fF cross-coupling**

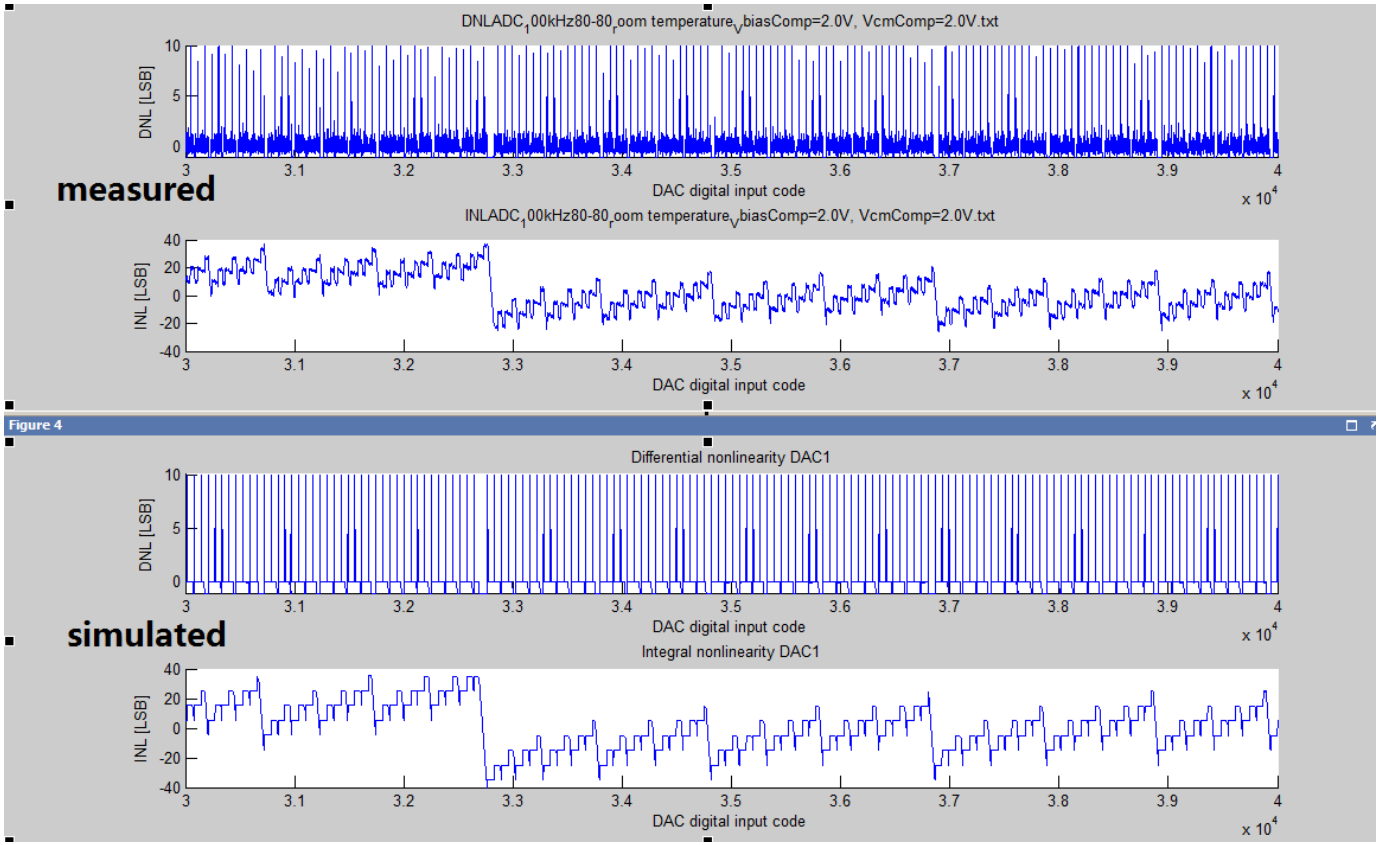






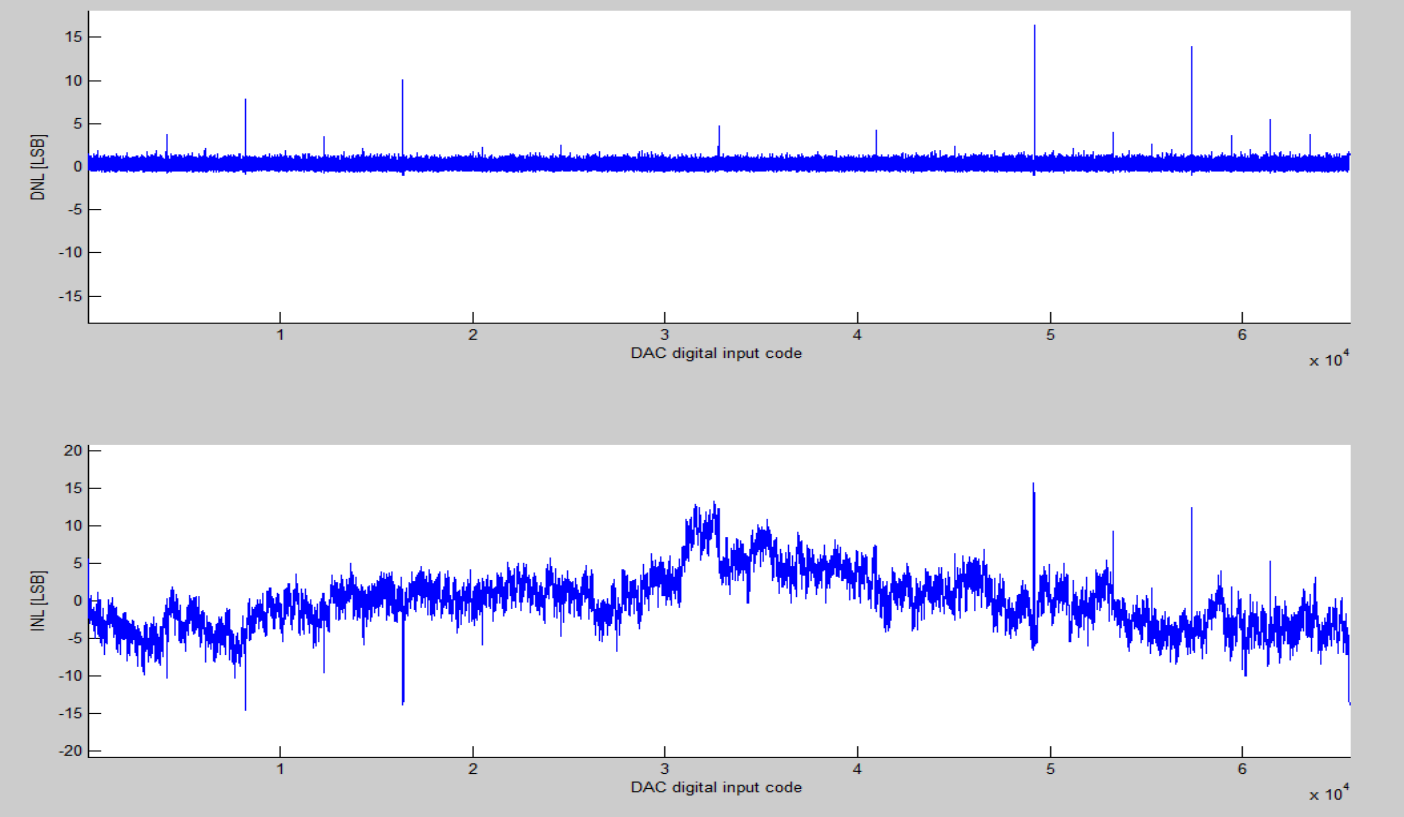
ADC INL DNL

- **ADC INL DNL problem analysis**



ADC INL DNL

- **ADC INL DNL @ 50KHz fs**



Measurement summary

Specs	Measurement result @ room T	@ cryogenic T
Supply voltage	3.5-3.6V	
Total current consumption	53mA	60.5mA
Regulator PSRR	> 40dB	
Regulator I out	> 40mA	
Output impedance	< 1Ω	
LDO output	1.3-3.4 V	
Analog rail to rail voltage	3.3 V	
Reference DAC INL	0.7LSB	1LSB
Reference DAC DNL	0.06LSB	0.04LSB
ADC noise	2.5LSB	2.1LSB
ADC fs	50, 100, 200KHz	
ADC INL	78LSB (15LSB@50KHz)	
ADC DNL	76LSB (16LSB@50KHz)	
Monitor resistance range	10KΩ -70KΩ	
Number of digital outputs/ inputs	32 / 8	
Digital output clock speed	0-10 MHz	
Serial interface speed	50KHz-50MHz	
SpaceWire bit rate	0-200 Mbps	
ASIC start-up time	≤50us	
Temperature range	77K-room T (Measured)	

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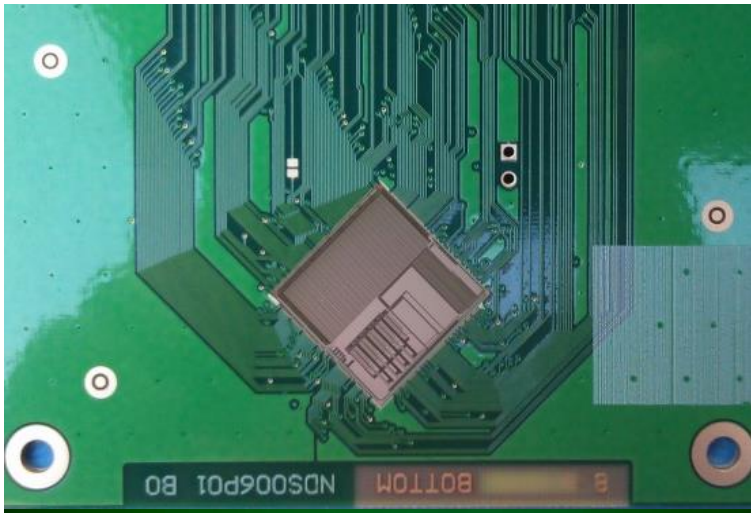

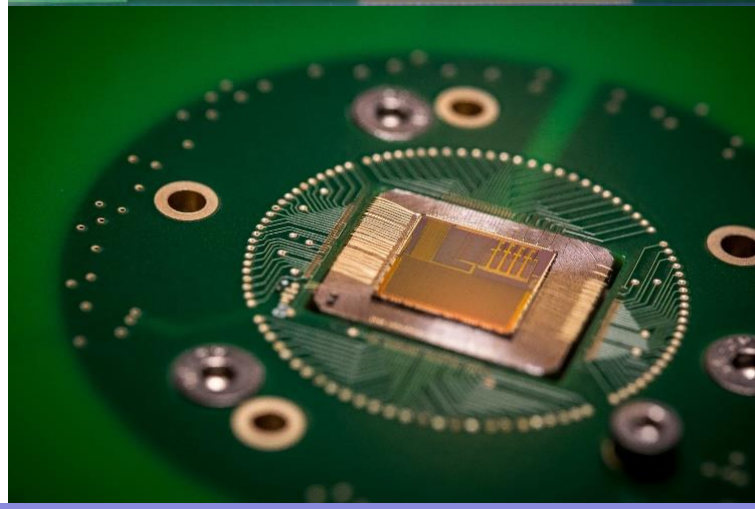

Conclusions

- Prototype accompany ASIC for (IR) detector arrays which provide all functionalities has been demonstrated
  - ADC problem founded and will solve in next iteration
- Full function has been proven from cryogenic (77K) to room temperature
  - All Caeleste custom designed cells
  - Digital cells in DARE Lib. Including SRAM
- Highly flexible for ROICs
  - Highly programmable sequencer
  - Wide programmability and large dynamic ranges in analog acquisition chain
- Beyond IR imagers

Next steps ?

- Larger ASIC with multiple channels (32 to 64)
- Faster ADCs is now developing at Caeleste (up to 12MS/s with reduced resolution)
- Irradiation testing
- More discussion with instrument builders and IR sensor manufacturers for further enhancements

Thank you!