Radiation hard design
in CMOS image sensors

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Outline

• Introduction

• Design for total dose
  ⇒ Total ionization dose TID
  ⇒ Displacement damage DD

• Design for single events
  ⇒ SEU single event upset
  ⇒ SEL single event latch-up

• Take home message
Introduction

About us
Background in Radhard CMOS design
About us

Founded 2006
Mechelen, Belgium
17p

Mission
and business model

Supplier of
Custom designed
Beyond “State of the Art”
Image sensors
Caeleste radhard background

Where we come from

⇒ Historical contribution to radhard and cryo design for space (ISOPHOT..., OISL, STAR250, HAS...)
⇒ Background in design for particle physics and X-ray integrating and photon counting detectors
⇒ Close relationships with foundry technologists
⇒ Expertise in circuit & device physics & technology

Present

⇒ Routine radhard design (TID, TnID, SE, SEL)
⇒ Proton & SE hard pixels
⇒ ROICs and image sensors
Heritage

OISL 2000
first >10Mrad

QX 2010
Analog domain 2-energy
“color” X-ray photon counting

ISOPHOT FIR ROIC 1989
SEU hard wo TR

1989
XYW event detector

1992
RD-19 SOI-CMOS

2013 wafer scale X-ray

STAR250/1000 2003
Disclaimer

- This paper focuses on design countermeasures, while understanding the damage mechanism itself.
- This is not a design course. Details of actual designs are not shown.
- Technology countermeasures, temperature effects, annealing not treated.
- No guarantee on effectiveness of techniques, nor of IP freedom.
TID: total ionizing dose
also referred to as IEL ionizing energy
loss

Introduction

total ionizing dose

TID total ionizing dose
DD displacement damage
SEU single event upset
SEL single event latch-up
Take home message
Radiation:

⇒ Primarily X, γ, but essentially all particles

Dominant effect:

⇒ Creation of positive space charge in the SiO2 (SiN) dielectric layers

⇒ Also: increase of interface states at Si-SiO2 interface

Effect on CMOS circuits:

⇒ Moderate shift of Vth, μ degradation and 1/f noise increase

⇒ Parasitic S-D leakage via STI/field in nMOSFETs resulting in large dissipation and malfunction
Effect on CMOS pixels:

⇒ Moderate offset shift and 1/f noise increase
⇒ Lateral shunting between pixels
⇒ Lower gain and increased PRNU
⇒ Increased average $I_{dark}$ and DNSU

Most publications are describing this last effect
Design countermeasures

- Buried diodes as the general way to reduce dark current
- Avoiding the parasitic source-drain leakage in nMOSFETs
- Several case-by-case other measures
TID-hard CMOS

Regular transistor
Leaks when STI/field inverts

Annular transistor:
No path over STI/field

H-gate transistor:
Leakage path over STI/field is blocked by P-implant
The “CES” IR ROIC

Fully radhard & cryo\textsubscript{77K}
UMC018
Digital: DARE library
Analog: CaelesteRH

$\gg 1 \text{Mrad, not tested yet}$

ESA consortium
Caeleste+Easics+Selex
2014
4 SAR ADCs, detail
Digital logic, detail
Caeleste RH library

CaelesteRH as compared to SotA

Available in 3 technologies, porting is standardized
Full analog & mixed mode
Very high TID & TnID hardness
Very high SEL hardness
Very high SEU hardness wo TR
<20% increased Cin and power
<50% area increase
TID Gamma
Radhard pixels

**LAP2010 device**
Tower TSL018
2011

TID of gamma $^{60}\text{Co}$

Compared to published SotA
TID Gamma ≠ Electrons

- LAP2010 device
  - Tower TSL018
  - 10 devices; many pixels per device

TID of
- 300keV electrons
- 1.2/1.3 MeV gamma $^{60}\text{Co}$

Effect on
- Buried PPD
- Surface FD
DD

displacement damage

also referred to as “NIEL” non-ionizing energy loss
Radiation:
  ⇒ HE particles: protons and heavier
Dominant effect:
  ⇒ Non-elastic displacement of Si atoms
  ⇒ Often creating an initial vacancy + interstitial
Effect on CMOS pixels:
  ⇒ Point-wise heavily leaking diodes, hot pixels
  ⇒ Often blinking “RTS” dark current pixels
Photodiode redundancy?

Proton/Neutron/other_particle

⇒ displacement damage in the photodiode creates “hot” or “RTS” pixel
⇒ SE creates flash

No way to remove or calibrate this?

Suppose we split the pixel in 2...100 parts. The defect will reside in only one

Redundancy?

⇒ Readout all, remove the defect part’s signal and average.
⇒ Take a weighted maximum voltage by winner take all circuit or sourcefollower
Photodiode redundancy

radhard design in CMOS image sensors
SEU

double event [upset]

Also SEE, SEFI, SET, SEGR, SEB ... ()

SEL is separately treated
Radiation

⇒ Sometimes X, γ, e-, but rather much heavier particles

Dominant effect:

⇒ Creation of instantaneous + or − charge packet sufficient to toggle a latch

Effect on CMOS and CMOS pixels:

⇒ register or memory loosing information
⇒ flash seen by the photodiode
The loss of bits in SRAM cells or Flip-flops
SEU

Mechanism

• Particle deposited charge packet charges one node of a latch to the opposite logic value
Flipping the inverter @t₀
Flipping the inverter @\(t_0+0.5\)ns

Hole drift/diffusion
Electrons drift/diffusion
SEU countermeasures

- Shield against particles
- Make vulnerable volume small
- Make vulnerable node capacitance large
- Triple (and other froms of) redundancy
- Detectability, read-back, re-upload
SEL

single event latch-up

SEL
Radiation
⇒ Protons and rather even heavier particles
Dominant effect:
⇒ Creation of instantaneous + or – charge packet sufficient to initiate a PNPN latch-up
Effect on CMOS:
⇒ Circuit collapsing and potential destruction due to excessive supply current
Bulk CMOS has an annoying thyristor

VDD

3.3

PNP

NPN

VSS

0
Bulk CMOS has an annoying thyristor
Thyristor = 2 * BJT

- Threshold for ignition: Q, C
- Conditions for sustaining: \( \beta, R \)

Attention: these two resistors are physically partly the same. This external element model is imperfect!
Quantitative compact (=SPICE) model?
⇒ Much better: a 3D device simulator.

What lacks: value for series resistances
⇒ Series resistances in E, B, C. Can estimate it from technology data.
⇒ Pay attention that “resistance” applies to majority carriers. Base resistance is thus over/underestimated and partly uncorrelated
⇒ Emitter and Base resistances partly overlap: Emitter current increases IR drop of Base.

What lacks: models of the parasitic BJTs
⇒ $\beta$: must eventually “measure” that. Start with default value (100...1000) for “qualitative” estimate.
Design countermeasures

Avoid ignition
⇒ minimize sensitive volume
⇒ maximize C/Q: increase node capacitances

Avoid sustaining
⇒ Maximally reduce the series resistance in the thyristor
⇒ Between the nWELL and pWELL: guard rings metallically tied to VDD/VSS

Avoid proliferation
⇒ nWELLs (actually the well not being the substrate) should be fragmented. So that the latchup remains confined: when one section latches, the general supply voltage does not collapse.
Design style

Classic CMOS design style

Metal guardring around wells

Rails in the middle
Mirrored rails
Technology measures

Avoid the thyristor
⇒ SOI, FinFET

Reduce the bipolar feedback
⇒ Poor BJTs
⇒ Trenches
⇒ Low sheet resistances
⇒ Epi wafers (p- on p++ or n- on n++): reduces 1 Base resistor
⇒ Increased recombination → reduces minority current and increases $I_{dark}$

Reduce the pick-up
⇒ Small charge collecting volume in the Bases
Triple well...

The number of *possible* thyristors increases
Good to know

nMOS-only or pMOS-only circuit parts cannot latchup.
A standalone BJT does not latchup
SEL and vulnerable nodes

⇒ How much charge is deposited on a vulnerable node
Vulnerable volume @t_0

VDD

VSS

H^+ proton
Vulnerable volume @t_{0} + 10ps
Vulnerable volume $@t_0+0.5\text{ns}$
Net node charge as function of time

- Substrate electrons diffuse into depletion layer then drift into nWELL
- Electrons diffuse to nWELL VDD tie
- Holes in nWELL diffuse into depletion layer then drift into substrate
- Holes drift out of depletion layer to substrate
- Electrons drift into nWELL

Event:

~10ps

~1ns
How to estimate Q?

LET linear energy transfer

Heavy ions are commonly described by amount of energy lost per unit track length = Linear Energy Transfer

Linear Energy Transfer

⇒ Energy loss per unit path length
⇒ dE/dx= MeV/cm
⇒ Divide by material density = MeV.cm²/mg
⇒ LET of 100 MeV.cm²/mg corresponds to charge deposition of 1pC/μm = 6E6 e⁻/h⁺

How does LET spectrum relate to the real space environment?

⇒ A measure for the heaviest ions/events that can be expected
⇒ Says nothing about number of particles or probability
e-h+ pairs per µm

100 MeV.cm²/mg ≈ 1pC/µm = 6Me-h+/µm

⇒ This is a linear function, thus 50 MeV.cm²/mg is still 3 million charges/µm.

For reference /µm

⇒ α: 4E6 eh, max @1MeV
⇒ H+: 30000 eh, max @80keV
⇒ β (and γ): <5000 e-h+

⇒ More energy: less charges!
Voltage drop
assuming instantaneous charge deposition

Minimal junction size and capacitance
⇒ 1fF & 1µm: 6000 e- = 1V
⇒ Electrons (hence gamma) cannot create $V_{\text{forward}}$
⇒ Protons can (marginally) ignite LU

Proton SEL hard junction?
⇒ 5fF & 1µm: 30000 e- = 1V. Yet, shallow angle?
Net node charge as function of time

- Maximum effect electron / gamma <1 GeV
- Maximum effect proton
- Maximum effect alfa
- LET 100 MeV cm$^2$/mg
- Worst case threshold for SEL

~10 ps vs. ~1 ns
Take home message

conclusions
CMOS imagers can be made hard against TID, SEL, SEU etc by design

⇒ TID: avoid field leakage
⇒ SEL: reduce bipolar feedback
⇒ SEU: vulnerable volume & circuit redundancy

Photodiode hardening for SE and displacement damage remains a question
• Photodiode redundancy?
Thank you