

# Fast Charge Transfer in 100 $\mu\text{m}$ long PPD Pixels

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## Abstract

In this paper we present a photodiode structure for fast charge transfer in narrow and elongated pixels. For applications requiring high frame rate and elongated pixels, charge diffusion in photodiode limits the transfer efficiency (transfer time  $< 1\mu\text{s}$ ). We solve this by creating an electrostatic potential gradient in the direction of transfer by exploiting the proximity effect of implanted regions on the pinning voltage. The proposed method is realized in a pixel with dimension of  $7\mu\text{m} \times 100\mu\text{m}$ . The method does not influence the quantum efficiency and uses a standard 0.18 CIS process.

## Introduction

The transfer efficiency from photodiode to floating diffusion (FD) in a pixel is dependent mainly on 2 factors. Firstly, the diffusion time of the charges in photodiode and secondly, the efficiency of transfer gate. The diffusion of charges becomes a significant issue in elongated pixels for applications with limited transfer time. The diffusion time constant of charges in the photodiode is proportional to the square of its length as shown in the log-log plot in Figure 1.

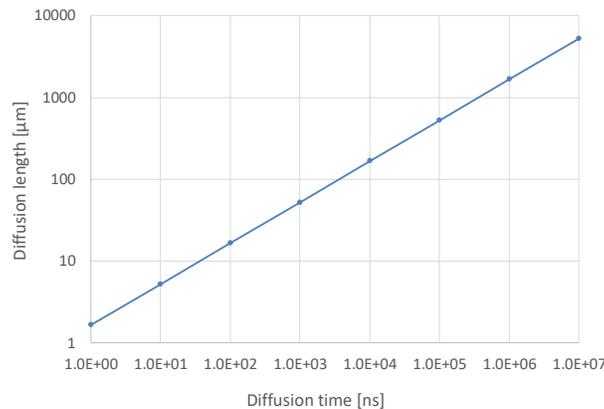


Figure 1: Diffusion length vs diffusion time of charges in photodiode

PPD design methods have been proposed in the literature to reduce the diffusion time by creating an electrostatic potential gradient in the PPD. The proposed methods employ the fact that the pinning voltage of the PPD is influenced by one or a combination of the below mentioned conditions.

1. Shape of the PPD implant [1,2,3,4]
2. Dose of the PPD implant [3]
3. Dose of pinning layer over the PPD implant or multiple epitaxial substrates [5]

The designs with PPD shape modifications suffers from lower sensitivity at narrower PPD widths while the designs requiring dose modifications require process modifications. The proposed method does not suffer from lower sensitivity as the PPD has a constant width and only a standard CIS technology is used.

## Pixel structure

In this section, the design methodology for the PPD is presented. The pinning voltage of a photodiode is influenced by the proximity of another implanted region. In this work, a standard P+ implant is used to influence the pinning voltage as shown in Figure 2. For a photodiode of constant width, the pinning voltage decreases as the P+ implant nears the PPD implant. The relationship between the pinning voltage and the gap between P+ and PPD implant follows the curve in Figure 3. Beyond certain values of the gap, the pinning voltage saturates.

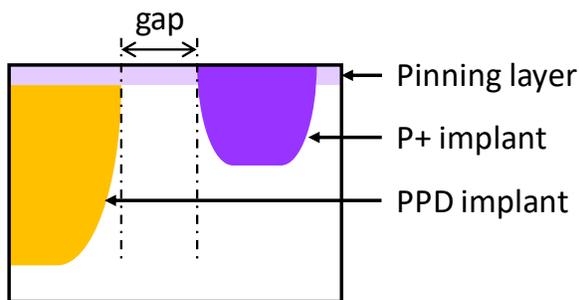


Figure 2: Cross-section view of photodiode with P+ implant

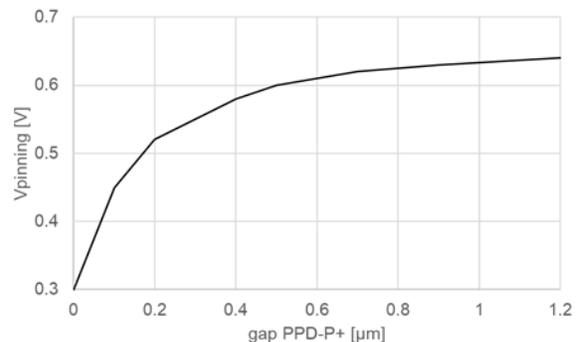


Figure 3: Vpinning of PPD vs gap

TCAD simulations confirm the concept. Figure 4 shows that the depletion region is restricted to a very small area when P+ region is touching the PPD implant. As the gap increases from Figure 5 to Figure 9 the depletion region is extended deeper and wider into the bulk silicon.

The gap between P+ and PPD implant is changed along the direction of charge transfer from PPD to FD such that a constant electrostatic potential gradient is

created. The potential gradient will ensure that charges undergo drift instead of diffusion. The resulting layout is shown in Figure 10.

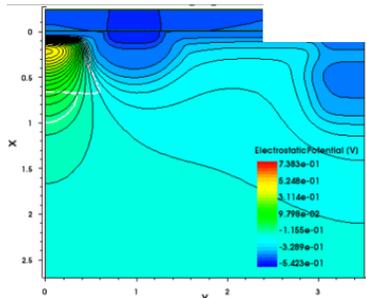


Figure 4: Gap = 0  $\mu\text{m}$

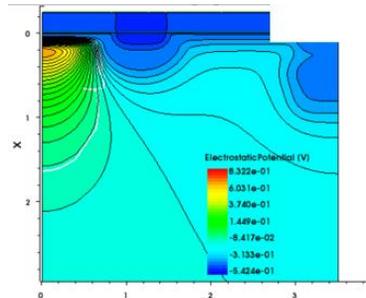


Figure 5: Gap = 0.2  $\mu\text{m}$

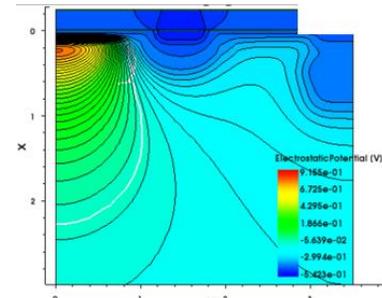


Figure 6: Gap = 0.5  $\mu\text{m}$

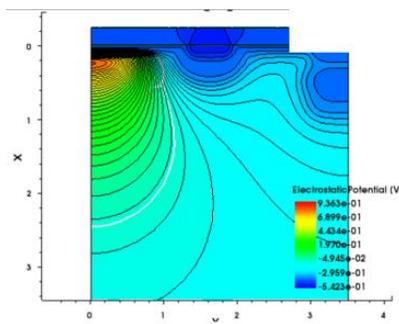


Figure 7: Gap = 0.7  $\mu\text{m}$

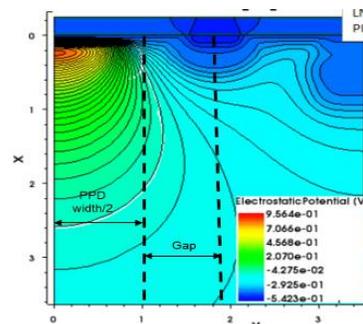


Figure 8: Gap = 0.9  $\mu\text{m}$

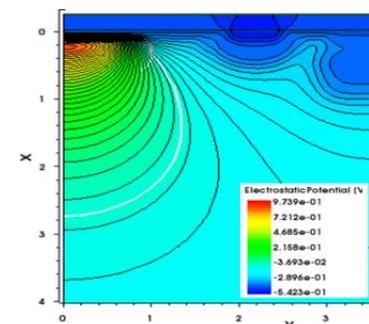


Figure 9: Gap = 1.2  $\mu\text{m}$

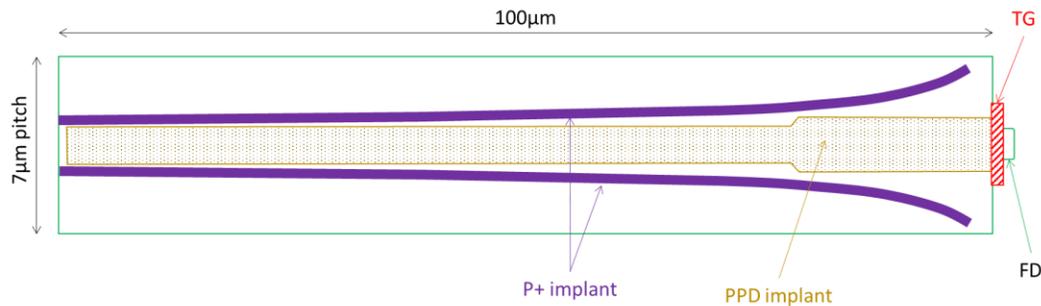


Figure 10: Layout of a 100  $\mu\text{m}$  elongated diode with P+ implant

## Measurement and Conclusions

The measurement results for the diode with and without P+ implant is shown in Figure 11. The position of the light pulse (width=0.6  $\mu\text{s}$ ) is moved closer to the falling edge of the TG ( $t=0$ ) for each measurement point. It can be observed that the potential gradient in the diode with P+ results in faster charge transfer compared to the diode without P+.

The shape and layout style does not influence the overall sensitivity of the diode as can be concluded from the quantum efficiency (QE) results in Figure 12.

Figure 13 shows the photo response measurement. It can be observed that under different pixel gain settings the charge handling capacity of the PPD is only limited in the lowest gain setting. The full well of the PPD is nearly  $800ke^-$ .

The concept can be extended to large square pixels without lowering the sensitivity of the pixels while improving the transfer efficiency.

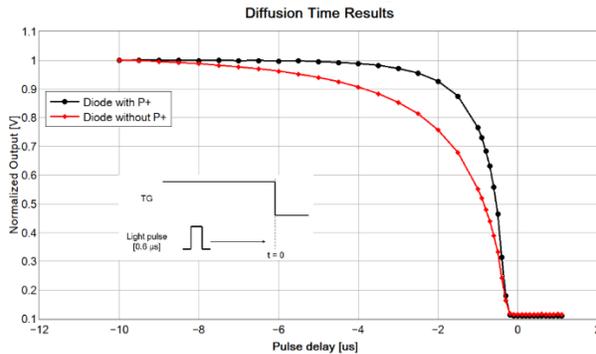


Figure 11: Diffusion time measurement result

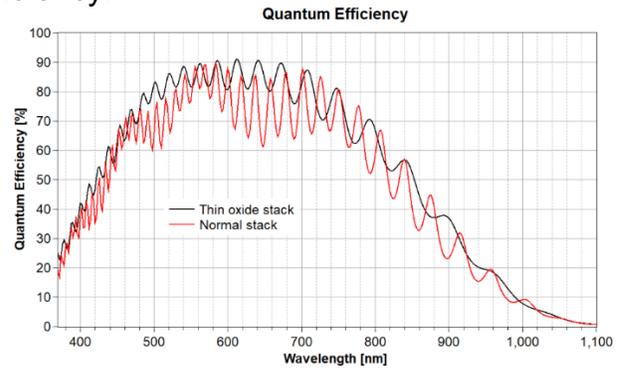


Figure 12: QE measurement. Red line: nominal diode, black line: same diode with dielectric layers partly removed.

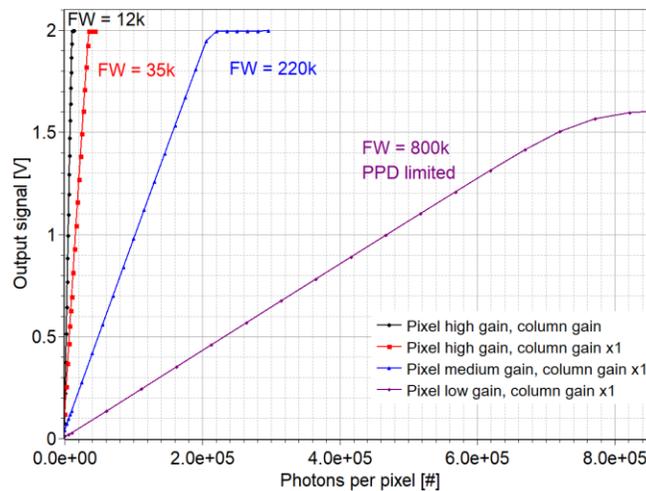


Figure 13: Photo response of the pixel with Full well indicated for respective gain setting

## References

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