CAE108 12-16 bit ADC

The 12-16 bit ADC8 is a standalone version of Caeleste's on-chip image sensor compatible SARADC family.

Features

- Conversion principle: Successive Approximation Register (SAR)
- 12 bit default nominal resolution
- 11 ENOB in 12 bit mode
- 14 bit and 16 bit resolution by in-ADC transparent oversampling, resulting in 12 and 13 ENOB
- TID, SEU and SEL radiation tolerant
- Accepts pseudo-differential, fully differential and single-ended signals with on-chip generated reference
- Input sample rate nominal 40 MHz
- Analog supply 3.3V
- Digital supply 1.8V
- differential LVDS / CML output at 480 Mbps nominal rate

Application

Companion ADC of space image sensors
Companion ADC of cryogenic image sensors
ADC for nuclear and hazardous environment inspection applications

The evaluation kit includes

- Ceramic packaged ADC8
- PCB board with socket
- Differential BNC input
- LVDS output
- Demonstration program running on PC via interface