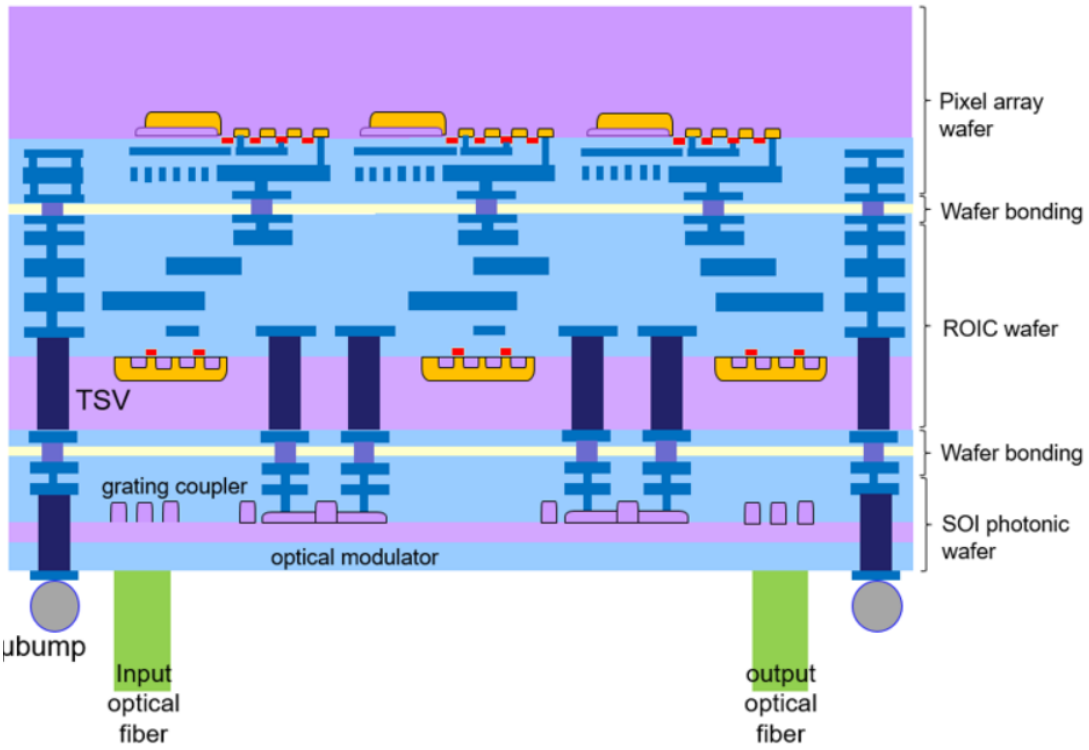
Caeleste CVBA
Hendrik Consciencestraat 1 b
2800 Mechelen, Belgium

Subject for Master Thesis & Internship

# Design of read-out layer for optically 3D stacked imager

The frame rate (images per second) of high-speed image sensors is today limited by the infrastructure needed to send the generated data out of a chip. The traditional, 2-dimensional, approach of putting rows of bond pads at all 4 edges of the die is reaching its limits in terms of number bond pads and the pitch between these bond pads.
A 3D approach of making image sensors is pioneered by the multinationals of consumer imaging (Sony, Samsung, …) and is now also becoming available in semiconductor foundries offering image sensor technology. This opens the way to use this technology for a 3D sensor optimized purely for frame rate.
Going even one step further[1], instead of sending the data out of the chip as electrical signals, one layer of this stack can be an opto-electrical or photonic IC that encodes the electrical signals onto a light stream that couples with an optical fiber.




The purpose of this study is to contribute to the design (concept, architecture, schematic and layout) of the different layers in this IC. Actual content is largely TBD en depending on the interests, skills of the candidate.

For further information or applications contact jobs@caeleste.be.

[1] G.Cai & al. “Photon to photon CMOS imager: opto-electronic 3D integration”, IS Americas, San Francisco, Oct 12-13 2017