Caeleste CVBA
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Subject for Master Thesis and Internship

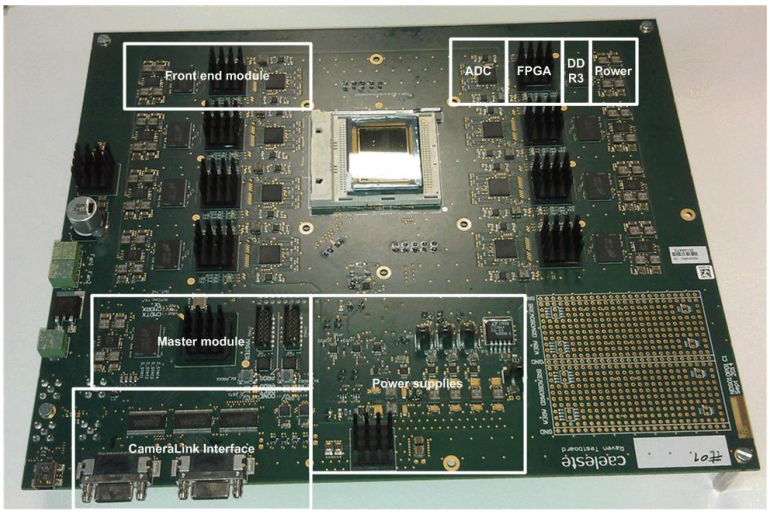
High-speed test system interface

Caeleste provides custom design of image sensors with very low noise, extreme dynamic range and/or extreme high speed. The systems to operate and test these devices are not available on the market as such and thus are designed and build by the Caeleste S&T team: a dedicated system for each project.

The time to construct a test system is limited: it is the time between the “tape-out” of a silicon design and the moment when wafers become available from the fab. This time is typically 3 months and in order to cope with this restriction, Caeleste test systems are built using as much as possible existing building blocks in hardware, firmware and software. These blocks are well-known, tested and found to be reliable.

One of these building blocks is the data interface between the test system and the computer. This data link has two components:

- A high-speed downstream data link: from the test system into the computer.
- A bi-directional command & control link to configure the test system, acquire housekeeping data etc.



Presently, the interface between the test system and a computer is done using the (somewhat older) CameraLink standard, allowing a maximum transmission rate of 5.6 Mbit/s. However, this connection has several disadvantages: it is bulky, requires dedicated hardware and a considerable software effort at the computer side.

In this master thesis we will improve all aspects of the interface. The work encompasses:

- Study of available standards for high-speed data transmission.
- A motivated choice of the standard to be used in future Caeleste test systems. This choice is made in close cooperation with the Caeleste S&T team.
- Hardware realization of all interface components at the test system side and, if required, at the computer side: schematic design, PCB layout, PCB production and assembly, testing etc. The purpose is to realize an operation-proven module that can be incorporated in future test system designs as a library component.
- Implement and test the required firmware in FPGA to support the high-speed data transmission at the test system side.
- Implement and test the software to support the data link at the PC side: drivers, DLL library components, example code, tutorial…

The thesis work includes a prior internship; the total duration of the thesis exceeds 6 man months.

For further information or applications contact jobs@caeleste.be.