European Low Flux CMOS Image Sensor

Description and Preliminary Results

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Outline

• Introduction
  • The ELFIS project
  • Need for charge domain Global Shutter (GS), High Dynamic Range (HDR) imaging

• The ELFIS image sensor
  • Sensor Floorplan
  • Target specifications and features
  • Charge domain GS HDR Pixel operation

• Test Setup
  • First Image

• Conclusions
Project Description

- ESA funded project “European Low Flux CMOS Image Sensor”
- Goal: to develop a Radiation hard, charge domain global shutter, high dynamic range pixel for low flux / high flux space applications

Project Partners

- LFOUNDRY: GS process development, wafer processing, backside thinning.
- AIRBUS: Electro optical characterization at 173K

Project duration: 30 months

- Start: Feb 2016
- End: August 2018

Project status: FSI Silicon
Need for GS, HDR Imaging
Voltage vs charge domain GS

- **Voltage domain GS method**
  - Voltage stored in an additional capacitor
  - High Dark current on FD results in High Dark Current shot noise (DCSN)

- **Charge domain GS method**
  - Electrons stored in a Storage node
  - DCSN reduced by surface pinning layer

[Diagram showing TG1, TG2, PPD, SN, FD, p-substrate]
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Sensor Floorplan

- **Control logic**
- **Rowdriver**
- **Control Logic & test overhead**
- **Column load**
- **Column and Video buffers**
- **Scanning Logic**
- **Single to Differential**

1920 x 1080
## Pixel Specifications

<table>
<thead>
<tr>
<th>Process</th>
<th>Lfoundry 110nm CMOS Image Sensor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pixel size</strong></td>
<td>15µm x 15µm</td>
</tr>
<tr>
<td><strong>Pixel array</strong></td>
<td>1920 x 1080</td>
</tr>
<tr>
<td><strong>Full Well</strong></td>
<td>High Gain: 7Ke-</td>
</tr>
<tr>
<td></td>
<td>Low Gain: 200Ke-</td>
</tr>
<tr>
<td><strong>Read Noise</strong></td>
<td>High Gain: 5e-</td>
</tr>
<tr>
<td></td>
<td>(nominal condition)</td>
</tr>
<tr>
<td></td>
<td>High Gain: 2.5e-</td>
</tr>
<tr>
<td></td>
<td>(low noise mode)</td>
</tr>
<tr>
<td></td>
<td>Low Gain: 110e-</td>
</tr>
<tr>
<td><strong>Shutter Mode</strong></td>
<td>Rolling Shutter</td>
</tr>
<tr>
<td></td>
<td>Integrate then Read(ITR)</td>
</tr>
<tr>
<td></td>
<td>Integrate While Read(IWR)</td>
</tr>
<tr>
<td><strong>Fill Factor</strong></td>
<td>100%</td>
</tr>
<tr>
<td><strong>CIS Type</strong></td>
<td>Backside Illuminated</td>
</tr>
<tr>
<td><strong>Quantum Efficiency</strong></td>
<td>&gt;50% 350nm – 800nm</td>
</tr>
<tr>
<td></td>
<td>&gt;90% peak</td>
</tr>
<tr>
<td><strong>MTF</strong></td>
<td>&gt;50% @ 1 Nyquist</td>
</tr>
<tr>
<td><strong>Dark Current</strong></td>
<td>&lt; 50 e/s/pixel @ 25°C</td>
</tr>
</tbody>
</table>
### Other Specifications

**CDS**  
Programmable on or off-chip CDS

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame rate</td>
<td>75 FPS @ GS HDR</td>
</tr>
<tr>
<td>Clock Speed</td>
<td>40MHz</td>
</tr>
<tr>
<td>Output Channels</td>
<td>16</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>700mW</td>
</tr>
<tr>
<td>TID</td>
<td>100 KRad</td>
</tr>
<tr>
<td>SEL</td>
<td>62 MeV.cm²/mg</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-100°C - +60°C</td>
</tr>
<tr>
<td>Packaging</td>
<td>COB</td>
</tr>
<tr>
<td>Stitch design</td>
<td>Stitchable up to wafer scale</td>
</tr>
</tbody>
</table>
GS HDR Pixel - Topology

- High Gain: TG1 - SN - TG2
- Low Gain-a: TG3a - Ca - Ma
- Low Gain-b: TG3b - Cb - Mb
- Low Gain-a, Low Gain-b are used for IWR operation
GS HDR Pixel - layout

Output:
Reset Signal, High Gain signal, Low Gain Signal
GS HDR Pixel – End of Integration

[Diagram showing the integration process with labels for M, CN, FD, TG1, TG2, TG3, PPD, SN, and VDDpix.]

- M
- CN
- TG3
- PPD
- TG1
- SN
- TG2
- FD
- VDDpix

5 December 2017
CNES Workshop 2017
GS HDR Pixel – PPD to SN

Diagram showing the connection of PPD to SN via TG1, TG2, and TG3.

Key elements:
- PPD
- TG1
- TG2
- TG3
- Storage node
- FD
- SN
- RESET
- VDD
- C

Legend:
- M
- CN
- VDDpix

Diagram details:
- Phi axis
- FD
- R
GS HDR Pixel – Reset Readout

![Diagram of HDR Pixel Reset Readout](image)

- **M**: Storage node
- **PPD**: Photodiode
- **TG1**: Transistor
- **TG2**: Transistor
- **SN**: Storage node
- **TG3**: Transistor
- **FD**: Float
- **VDD**: Supply voltage
- **VDDpix**: Pixel supply voltage
- **Select**
- **RESET**

**Timestamps:**
- 5 December 2017
- CNES Workshop 2017
GS HDR Pixel – High Gain Readout

Next \( t_{int} \)

PPD

TG1

SN

TG2

Storage node

FD

TG3

C

RESET

VDD

Select

output

“S1”
GS HDR Pixel – Low Gain Readout

- PPD
- TG3
- FD
- VDDpix
- SN
- TG2
- TG1
- M
- Next $t_{int}$
- FD
- CN
- RESET
- VDD
- Select
- “R2”
- Storage node
- CG
- Merge
- C

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Test Setup
Test setup
Operation mode: Global Shutter, High Gain
Conclusions

• First preliminary result with New Charge domain GS process
• Fully European supply chain
• True GS, fully synchronous HDR pixel is realized for various process conditions

• Future work
  • GS Process evaluation by various process splits
  • Finishing BSI wafers
QUESTIONS?

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Backup slides
High $Q_{FW}$ range:
$DR=200000/50=4000:1$

Low $Q_{FW}$ range:
$DR=7000/2=3500:1$

Combination
$DR=200000/2$
$=100000:1$ 100dB