Rad-hard image sensors
area/power/hardening trade-offs

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Outline

• Motivation
• A short summary of radiation effects
• A short summary of counter measures
• Countermeasure effect on area, speed and power
• Take home messages
Chapter 1

MOTIVATION
Purpose

- Overview of actual radiation hard circuits
- Direct comparison with the non-radhard equivalents.
- For image sensors and their periphery circuits.
- Focus on different type of radhardness and their impact on area, speed and power

- *Not* touch the actual hardness levels achieved nor pixel radhard design
Example

A common logic block: different level of radiation hardness. As each of these are different in approach and effect, this is rather a case study than a systematic overview.

Non-radhard

TID+SEL hard

SEU+SEL hard (TR)

Both combined
SE hard and not TID hard?

It is perfectly possible – and this actually makes sense – to design purely for SEL (single event latch-up) hardness, and disregards the other forms of hardness.

SEL hardness usually does not require a large area penalty in image sensors, whereas for many mission types it is the only damage mechanism that may be threatening for the mission.
Chapter 2

SHORT SUMMARY OF RADIATION EFFECTS
Van Allen belts:
High-energy electrons and protons
Trapped in the Earth’s magnetic field

Outer Belt
12,000 – 25,000 miles

GPS Satellites
12,500 miles

Inner Belt
1,000 – 8,000 miles

Low-Earth Orbit (LEO)
International Space Station
230 miles

Geosynchronous

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From: V.Huard, “Enabling space applications in advanced CMOS nodes: challenges and opportunities”, March 1, 2016
SEE (Single event effects)

- SEU single event upset
- SEL single event latch-up

There exist many more “SE”s, such as SEGR

- Which are typically rare or irrelevant in CMOS
- Have no countermeasure except shielding or the SEU/SEL counter measures already in place
Corruption of bit in SRAM or Flip-flop

⇒ Charge packet deposited by particle charges
⇒ One node of a latch to the opposite logic value

Electrons

1

0

1

0

0

1
High energy particles tuned on the parasitic thyristor of bulk silicon

⇒ power supply shorts
TID (total ionizing dose)

Radiation:
  ⇒ X, γ, charged particles

Dominant effect:
  ⇒ Positive space charge in dielectric layers
  ⇒ Increase of interface states at Si-SiO₂

Effect on CMOS circuits:
  ⇒ Moderate degradation of Vth, μ and 1/f noise
  ⇒ Parasitic S-D leakage in nMOSFETs
Chapter 3

SHORT SUMMARY OF COUNTER MEASURES
TID-hard nMOSFET
avoid the parasitic S-D leakage

Regular transistor
Leaks when STI/field inverts due to positive charge built-up due to ionizing radiation

Annular transistor:
No path over STI/field

H-gate transistor:
Leakage path over STI/field is blocked by P-implant
TID countermeasures

- Shield against radiation
- Ring MOSFETs
- H MOSFETs
- SOI/FINFET
- Defensive circuit design

<table>
<thead>
<tr>
<th></th>
<th>Adequate</th>
<th>Helps</th>
<th>Minor effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shield</td>
<td>★★★★</td>
<td>★★★★</td>
<td></td>
</tr>
<tr>
<td>Ring</td>
<td>★★★★</td>
<td>★★★★</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>★★★★</td>
<td>★★★★</td>
<td></td>
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<tr>
<td>SOI/FINFET</td>
<td>★★★★</td>
<td>★★★★</td>
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<td>Defensive</td>
<td>★★★★</td>
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</tbody>
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SEU
Design countermeasures using TR

Triple-redundant-slave flipflop
SEU countermeasures

- Shield against particles
- Make vulnerable volume small
- Make vulnerable node capacitance large
- Triple (and other forms of) redundancy
- Detectability, read-back, re-upload
SEL
Design counter measures using guard rings

Classic CMOS design style

Metal guardring around wells

Rails in the middle
SEL countermeasures

Avoid ignition

⇒ Reduce pick-up: minimize sensitive volume
⇒ maximize C/Q: increase node capacitances
⇒ No thyristor: SOI, nMOS only, FINFET

Avoid sustaining

⇒ Reduce the series resistance in the thyristor
⇒ guard rings metallically tied to VDD/VSS

Avoid proliferation

⇒ Fragment nWELLs
⇒ Detect & reboot
Chapter 4

LAYOUT EXAMPLES
(A)SPI register

- Static register with (here)
  - 3 address bits
  - 3 databits

- TID-hard, SEL-hard
  - TID-hard databit

- SEU-hard by TR data register, SEL-hard, not TID-hard

Xfab XS018
IO rail RDAC

TID, SEU and SEL hard
IO rail programmable bias

TID, SEU and SEL hard
IO analog buffer

TID and SEL hard
Cost of hardening

TR slave:
Area x 1.5
TR full
Area x 2
For register part

SEU-hard
• Not TID hard
• No specific SEL precautions
• TR in register bit slaves

“normal”
• Not TID hard
• No specific SEL precautions
• No TR

Area x 1.0 … 1.5
Power x 1.0 … 1.5
Speed x 1.0 … 0.5

TID-hard
• Specific TID countermeasures
• SEL countermeasures

TID&SEU
• Specific TID countermeasures
• SEL countermeasures
• TR in register bit slaves
Chapter 5

TAKE HOME MESSAGE
Take home message

Total Dose (Ionizing and Displacement damage)
  ⇒ High radiation hardness can be designed for
  ⇒ Weak points remains $I_{\text{dark}}$

Single Events (mainly SEU and SEL)
  ⇒ Nearly perfect protection against SEU and SEL can be designed for.
  ⇒ Remains weak for: very heavy ions
  ⇒ Inherent weak point: the pixel itself is made to detect radiation.

Independent TID and SEE hardness
  ⇒ Can be independent implemented.
  ⇒ Trade off depends on mission type, duration, shielding conditions, FEE intelligence...
References

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Thank you!