CMOS image sensor reaching 0.21 e- RMS read noise by inversion-accumulation cycling and oversampling

Recently Caeleste designed and evaluated a 0.18 µm technology 16*16 pixels (4 kinds of pixels) prototype CMOS image sensor with a measured read noise reaching 0.21 e^-_{RMS}. This result is obtained by the combination of oversampling and inversion-accumulation cycling.

In this image sensor, 4 kinds of pixels are designed: pixel with thick/ thin gate oxide wide/narrow pmos amplifier.

Results and Interpretation:

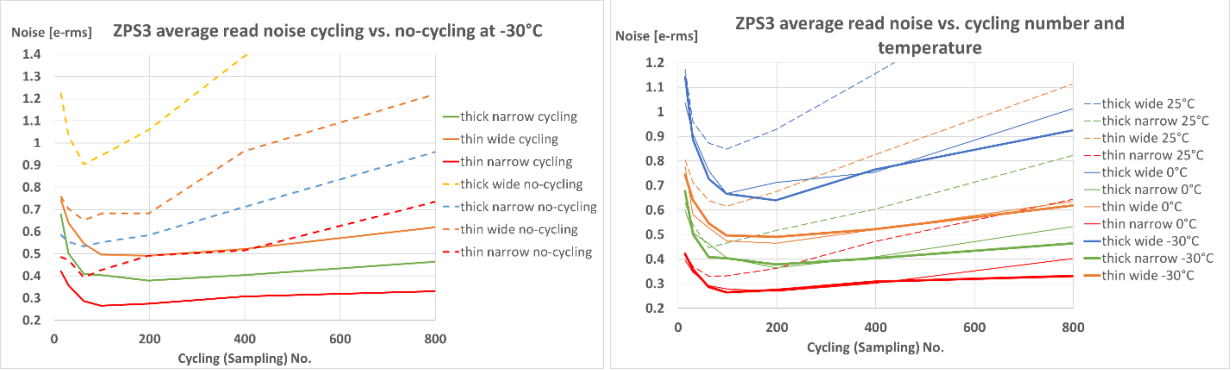

Figure 1, (left) average read noise cycling vs. no-cycling at -30 °C, (right) average read noise vs. cycling number and temperature

- Inversion-accumulation cycling helps to "laundry" flick noise to white noise [1], which can be easier decreased by oversampling.
- Oversampling decreases the white noise when sample number goes from low to middle (around 100).
- Integrated shot noise becomes the dominant noise source when sample number goes from middle to high. Lower temperature decreases integrated shot noise.
- Pixel with thin gate oxide narrow pmos amplifier has the lowest noise, because of the largest CVF.

Because of process variation, even the same kind of pixels has some noise difference. For pixels with thin gate oxide narrow pmos amplifier, the best pixel can reach 0.21 e^-_{RMS} read noise.

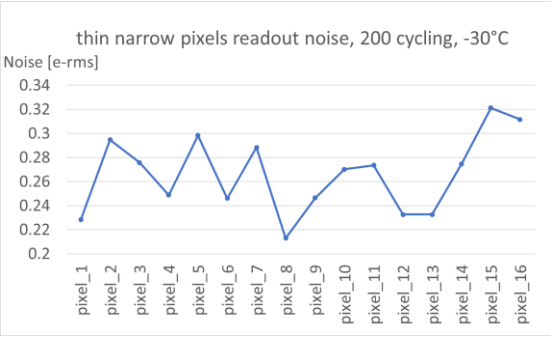

Figure 2 Read noise of different pixels with thin gate oxide narrow pmos amplifier

[1] B. Dierickx, N. Ahmed, B. Dupont, "A 0.5 noise electrons RMS CMOS pixel," Workshop on "CMOS detectors for high performance applications", Toulouse, Dec, 6, 2011.