A method to increase DR using column-level automatic gain selection

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Introduction

In this paper we present an image sensor with a very high linear dynamic range that is obtained by combining a pixel with using *three level transfer gate* method and a column-level automatic gain selection. The automatic gain selection (AGS) picks one out of three linear ranges each having a largely different conversion gain. The data rate remains the same as without high dynamic range, thus preserving the maximal frame rate.

Scientific CMOS (sCMOS)[1] uses dual column level amplifiers with different gains, dual ADCs and combine dual output data afterwards. In contrast here, we implemented the AGS function within the column readout circuitry, selecting one out of the three different conversion gains. The different conversion gains are realized in the pixel (large Q_{FW} and small Q_{FW}), and in the column amplifier having a gains 8x and 1x.

Three level TG method

The pixel topology is shown in Figure 1. One recognizes the classic 4T or 5T pixel, with an additional switch ("Merge") to a large storage node "C". The transfer gate TG can be biased at three different levels. TG2 is the electronic shutter or "flush" gate to adjust the integration time.

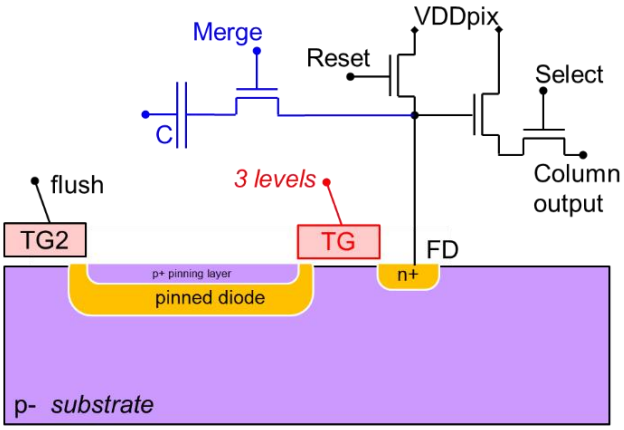

Figure 1 Three level TG HDR pixel

The operation principle is explained in the potential diagram and timing diagram in Figure 2. Initially both FD and the capacitor "C" are reset, then TG is biased at an intermediate level. Under low illumination level, the photo charges still stay in the pinned photodiode PPD. Under high illumination level, photocharges overflow to FD and "C" and a fraction of charges stays in the PPD. Initially, the Merge switch is turned off and the FD voltage level is sampled as value "R1". Then TG is toggled high – low, causing all photo charges left in the PPD to transferred to the FD; this new FD voltage level is samples as value "S1" – note that the difference "R1-S1" is a CDS. Next the Merge transistor is turned on again, the charges will be shared over the FD and the capacitor "C", and this voltage is sampled as value "S2". An external voltage 'Vblack' will be used as reference level for "S2".

Automatic gain selection

It would be possible to read out both differential signals (i.e. one high conversion gain CDS signal "R1-S1" and one low conversion gain non-CDS signal "Vblack-S2"), and re-create the HDR image off chip using these data. In order to increase the frame rate, a novel column readout circuitry with automatic gain selection (AGS) as shown in Figure 3 is implemented to reduce the output data volume. The AGS selects one of the

two differential signals coming from the pixel, or a third signal which is an 8x column amplified copy of the high gain signal.

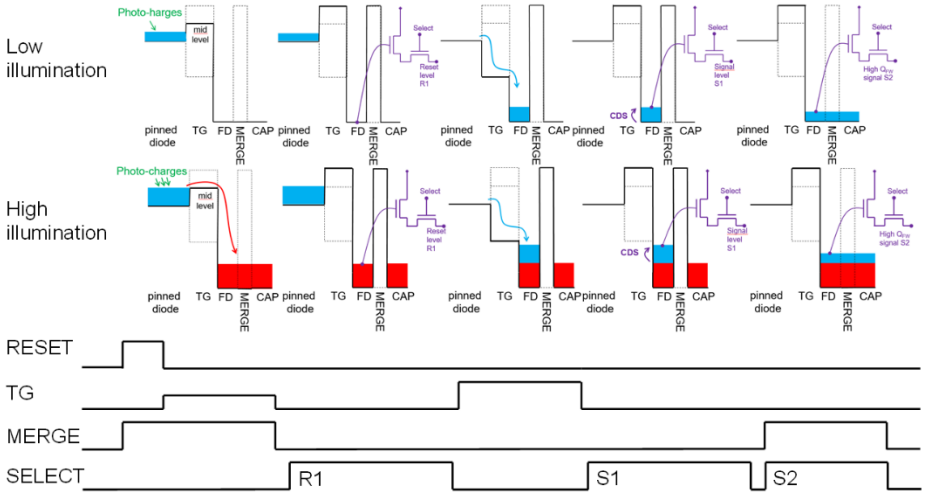

Figure 2 Potential diagram under low and high illumination level, and Timing diagram

The pixel's output signal on the column wire is readout through two column amplifier paths simultaneously: $Columnpath_1$ and $Columnpath_2$. The $Columnpath_1$ consists of a column amplifier "Amp1" which has a programmable gain "k" (normally set to 8x), a comparator whose one input is connected to Amp1 and another input is connected to a programmable reference "$Vref_1$", two sample and hold (S&H) capacitors (one samples R1, another samples S1), two multiplexing buffers which are connected to two analog buses (i.e. "RST_bus" and "SIG_bus") respectively, a latch to save the decision of the comparator and glue logic. The structure of $Columnpath_2$ is similar to $Columnpath_1$. The differences are that the column amplifier "Amp2" has a fixed gain equal to 1, one S&H capacitor can sample S1 or S2, an extra voltage reference "Vblack" and an extra multiplexing buffer is needed. Three different "RST-SIG" pairs, i.e. "$R1 \times k - S1 \times k$", "$R1 - S1$" and "$Vblack - S2$", and corresponding three signal ranges, i.e. high gain (HG), medium gain (MG) and low gain (LG), can be generated by combining this column readout circuits with the three level TG pixel.

The comparator in $Columnpath_1$ compares "S_1*k" with "$Vref_1$" and the comparator in $Columnpath_2$ compares "S_1" with "$Vref_2$". Based on the comparator result, the AGS circuits will determine which one of the three available differential signals to put on the "RST_bus" and "SIG_bus". The analog signals can be multiplexed to the two analog buses and converted by 12-bit on-chip ADC. The digital gain selection bits, i.e. AGS<1> and AGS<2>, will also be sent out to the serializer together with the conversion results from the ADC, then to the LVDS channel. The table below shows which signal to be found on the video buses

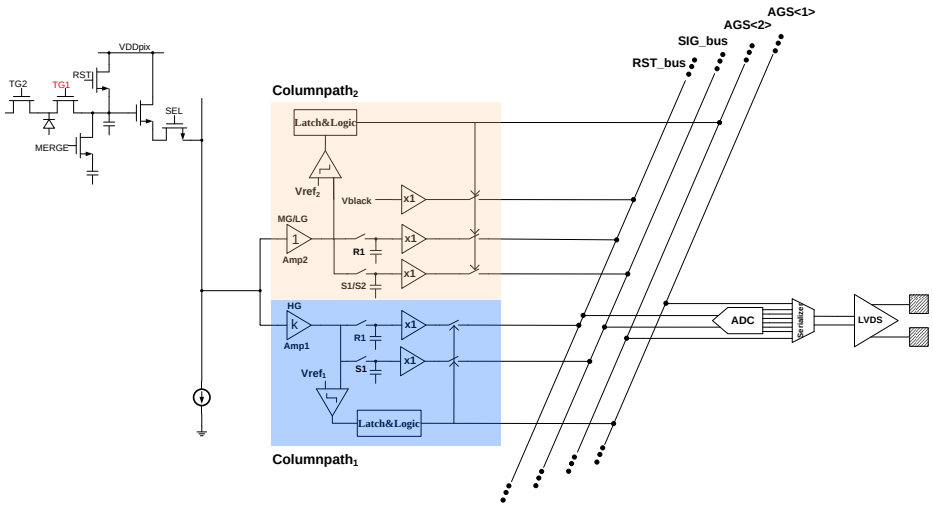

Figure 3 Column readout circuit with automatic gain selection

under which condition.

Comparator Condition	AGS<1,2>	RST_bus	SIG_bus	Which columnpath is selected
S1 x k > $Vref_1$	11	R1 x k	S1 x k	$columnpath_1$ (HG)
$Vref_1$ / k > S1 > $Vref_2$	01	R1	S1	$columnpath_2$ (MG)
S1 < $Vref_2$	00	Vblack	S2	$columnpath_2$ (LG)

Measurements

Figure 4 shows the quantum efficiency of the sensor. Figure 5 and Figure 6 show the photo response curve and noise of three ranges respectively. Figure 7 shows the raw HDR image and corresponding gain map (HG: red, MG: green, LG: blue) and Figure 8 shows the synthesized HDR image with histogram equalization. Table 1 summarizes the sensor performance.

References

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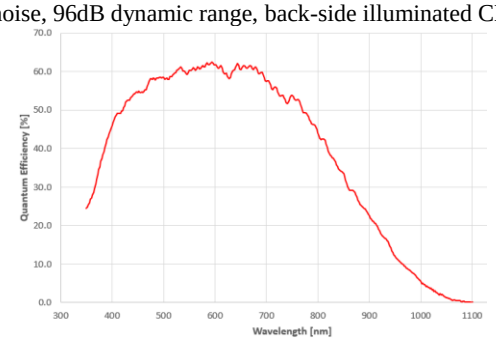

Figure 4 Quantum efficiency

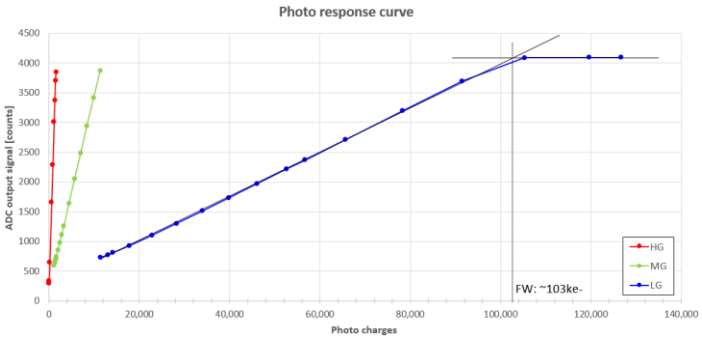

Figure 5 photo response curve over full DR with AGS

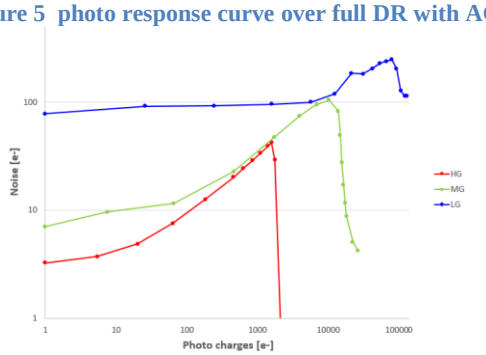

Figure 6 Noise in three ranges (T_{int}=20ms, room temperature)

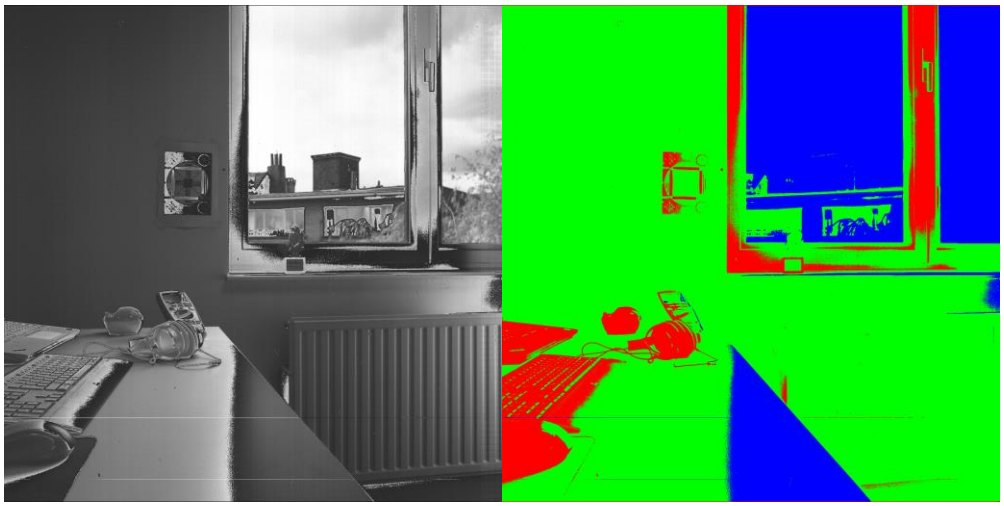

Figure 7 High dynamic range image (left: raw analog data, right: 3-gain map)

Figure 8 Synthesized HDR image with histogram equalization

Table 1 Sensor performance

Sensor performance	
QE	62% at 600nm
Full well (e-)	103k
Temporal noise (e-)	2.5
Linear dynamic range	92dB
Black sun	No black sun
ADC	On-chip 12bit ADC
Output data	12bit+AGS<1,2>