CRYOGENIC AND RADIATION-HARD ASIC FOR INTERFACING LARGE FORMAT NIR/SWIR DETECTOR ARRAYS

Peng Gao[1], Benoit Dupont[1], Bart Dierickx[1], Eric Müller[1], Geert Verbruggen[2], Stijn Gielis[2], Ramses Valvekens[2]
[1]CAELESTE, Mechelen, Belgium. [2]EASICS, Leuven, Belgium

I. INTRODUCTION

For scientific and earth observation space missions, weight and power consumption is usually a critical factor. In order to obtain better vehicle integration, efficiency and controllability for large format NIR/SWIR detector arrays, a prototype ASIC is designed. It performs multiple detector array interfacing, power regulation and data acquisition operations inside the cryogenic chambers. Both operation commands and imaging data are communicated via the SpaceWire interface which will significantly reduce the number of wire goes in and out the cryogenic chamber. This "ASIC" prototype is realized in 0.18um CMOS technology and is designed for radiation hardness.
In this paper we will describe the design, manufacture and test results of this device. In section II the architecture of the "ASIC" will be introduced. Some key building clocks will be shown in section III. Design style against environmental issue such as space radiation and cryogenic temperature will be mentioned in section IV. The test result and its improvement will be discussed in section V, followed by a section on conclusions and future work.

II. SYSTEM AND ASIC ARCHITECTURE

In a typical imaging system, apart from the sensor itself, the peripheral electronics typically consist of 3 parts: digital control, analog bias and data acquisition, and power supplies. In this ASIC, all these relevant functions are integrated on-chip. In the cryogenic environment, interfacing only to the unregulated power supply and the controller/processor sending commands to and receiving image data from the ASIC over Spacewire, and interfacing to other room temperature digital processors.
The ASIC functional diagram is shown in Fig. 1 [1]. The upper right part indicated as "supplies" are the on-chip LDO power regulators taking the unregulated (possibly unstable and noisy) power and providing a stable clean voltage for the detector and other functional sections. The "analog part" (upper left) digitizes the image data and generates a number of the bias voltages for the detector. The "digital part" at the bottom provides the control pulses to the detector and on-ASIC analog modules. Each section will be described in detail hereafter.

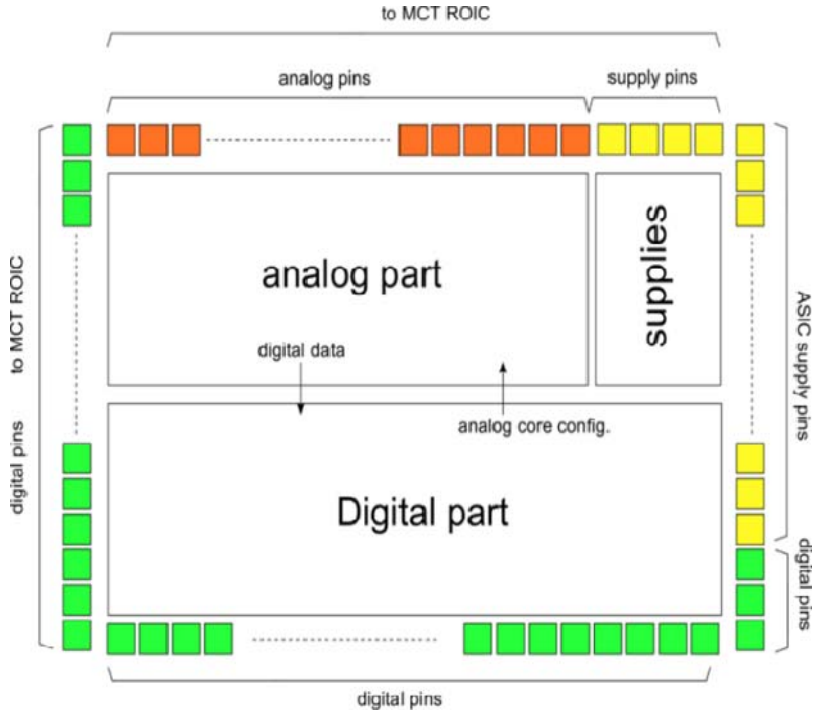

Fig. 1: ASIC floorplan

A. Supply section

Usually, an electrical system need power supply domains to isolate the noisy digital part from the clean analog domains. Typically these multiple power supplies are regulated from a common "unregulated" DC supply. As the detector and analog sections need several clean and stable power supplies there will be multiple regulators as closes as possible to the cryogenic chamber. This compromises the cooling power, still remains vulnerable to pick noise due to the long interconnects. The ASIC's on-chip LDO regulators reduce the amount of external supplies to the minimum and also relaxes the requirements of the external power supply quality. The drawback that the regulators generate heat inside the cryogenic chamber is minimized using LDO (Low Dropout) regulators. Although the relevance of a regulator inside the cryostat remains questionable in terms of power dissipation, the programmable power supply will be useful for many applications where component area is a concern

This prototype ASIC contains 4 identical LDOs (figure 2). Each of them can output a regulated voltage from 1.3-3.4V which can be programmed with a voltage step size of about 10mV. The maximum output current is 40mA per LDO.

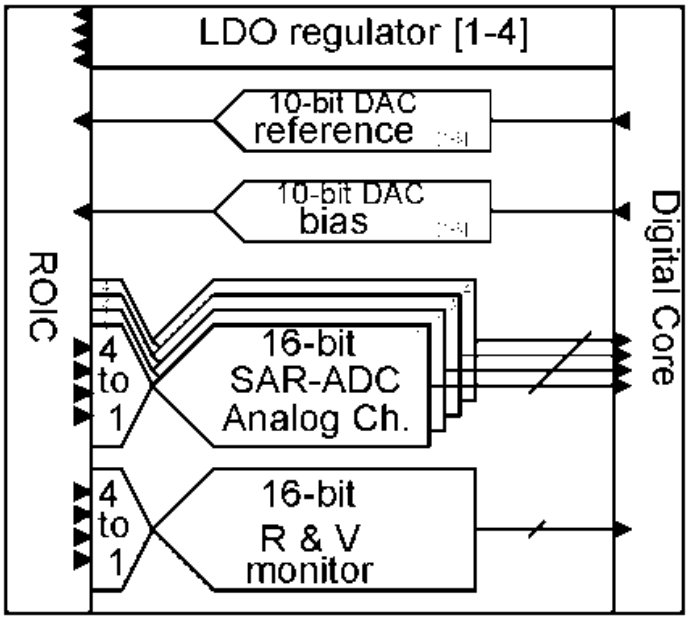

Fig. 2: Analog and supply sections diagram

B. Analog section

The analog periphery of a typical image sensor system does the analog to digital conversion of the analog data and generate the bias or reference voltages required by the detector ROIC. The analog building blocks of this prototype ASIC are depicted in Fig. 2. Four 16-bit ADCs convert 16 analog input channels via four 4-to-1 analog multiplexers. Such configuration is a reduced set compared to the full scale device to be designed for the future, where more ADCs will be implemented and not using the multiplexers. Fig. 3 shows one analog channel. The 4 to 1 multiplexer is followed by the CDS stage which can be by-passed. A programmable gain and offset amplifier adjusts the signal range to the ADC input dynamic range and may cancel the channel-to-channel offset. The actual ADC operates up to 100 KHz sampling frequency.

In order to properly bias the detector, sixteen 10-bit programmable voltages DACs are available. A rail-to-rail buffer is added to each DAC that can allow the reference voltages to drive a certain capacitive load.

Furthermore 4 monitoring channels which can be reconfigured to either monitor differential analog input voltage or the resistance of a resistor. This is particularly useful to monitor temperature and health status of various parts of an instrument. In order to measure the resistance, an on-chip switched-capacitor current reference is designed, whereby the applied clock frequency determines the useful resistance measurement range.

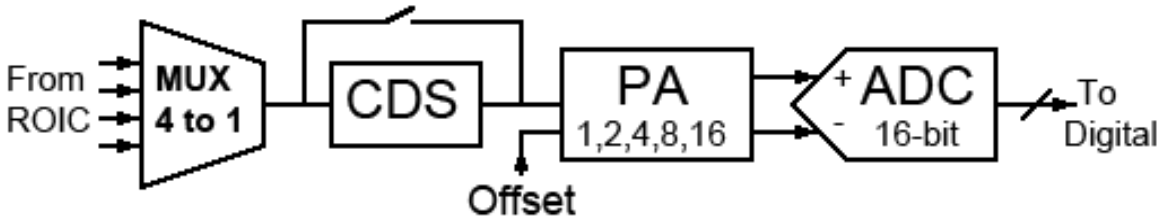

Fig. 3: One analog channel

C. Digital section

The digital part is essentially the highly programmable sequencer, the clock/reset generator, and the interface block. It provides the control signals to the detector array, to the analog signal processing, the reference clock of the monitoring ADC, and communication links via SpaceWire up to 200Mbit/s. The digitized image data is packaged and transferred on the same communication link. A low speed SPI was added towards the imagers addressing the need of certain vendors, thus making the ASIC more versatile.

The core of the digital section is the timing generator. In this prototype, 32 digital channels are placed in a flexible scheduler. The granularity of the sequencer is in this prototype 100ns, implying that the fastest driving signal can have a frequency of 5MHz. The user can define macros in the sequencer and call them from a master sequencer. The nesting depth of sequences in this prototype implementation is seven. From implementation standpoint, the sequencer is uploaded once via the SpaceWire interface in the device memory. As SRAM cells had not been de-risked at cryogenic temperature before the design phase, this prototype also embeds as back-up a classic but smaller register file. In the meantime the cryogenic operation of this SRAM was proven on this ASIC.

Fig. 4 shows the block diagram of the digital sections:

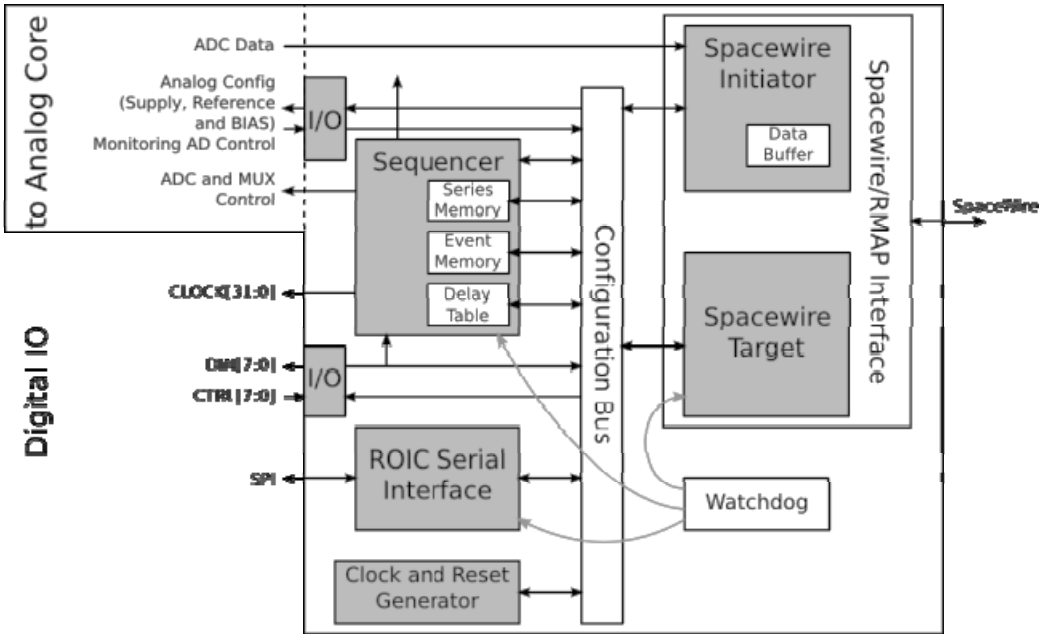

Fig. 4: Digital section diagram

III. BUILDING BLOCK DESIGN

Some of the key building blocks design will be discussed in this section.

A. LDO

The block diagram of the LDO is shown in Fig.5. The low dropout regulator uses a pMOS transistor as its pass gate which allows minimal headroom, down to about 0.2V. In such circuit special attention was paid during design to the stability of the circuit, since the circuit contains a feedback loop over two inverting amplifiers, resulting in a closed loop frequency response with two low-frequency poles, one due to the large pMOSFET gate capacitance, the other due to the external load capacitor. Therefore, we had to compensate one of the two poles. We used the ESR (equivalent series resistance) concept used to stabilize the loop [2].

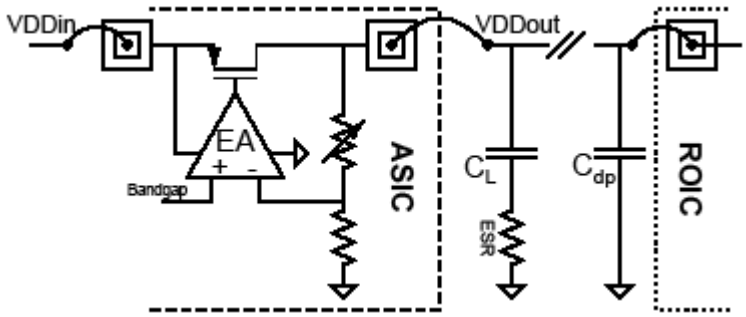

Fig.5: LDO schematic

B. ADC

The 16-bit ADC is another challenging building block on this ASIC. Its diagram is shown in Fig. 6.

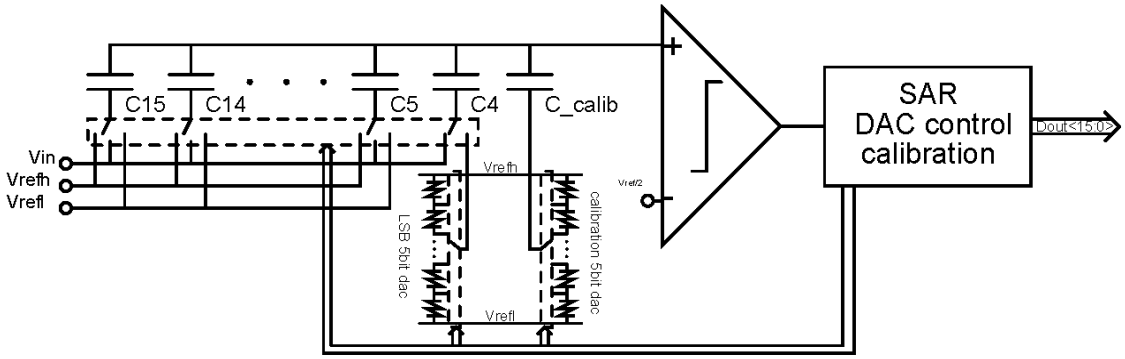

Fig. 6: ADC schematic

The successive approximation (SAR) ADC uses a hybrid topology to limit the input capacitance as well as to recover from the imperfect matching in the capacitor bank. The 16-bit resolution is split up in an 11-bit binary capacitor bank and a 5-bit resistive division sub-DAC [6]. In order to achieve the required resolution within the limited Silicon area and power budget, sizes are limited, hence matching is imperfect and calibration is necessary. As shown in Fig. 6, a calibration capacitor (C_calib) is connected between a resistor DAC and the main capacitor bank. At the startup of ADC [3], the actual mismatch between capacitors must be measured and then calibrated during the normal bit cycling. Comparator auto-zeroing is applied to reduce the offset error below LSB/2. To estimate the number of bits required for the calibration a model-based approach was developed. The following diagram shows the effect on DNL of a multi-bit calibration per stage for different Monte Carlo runs [4].

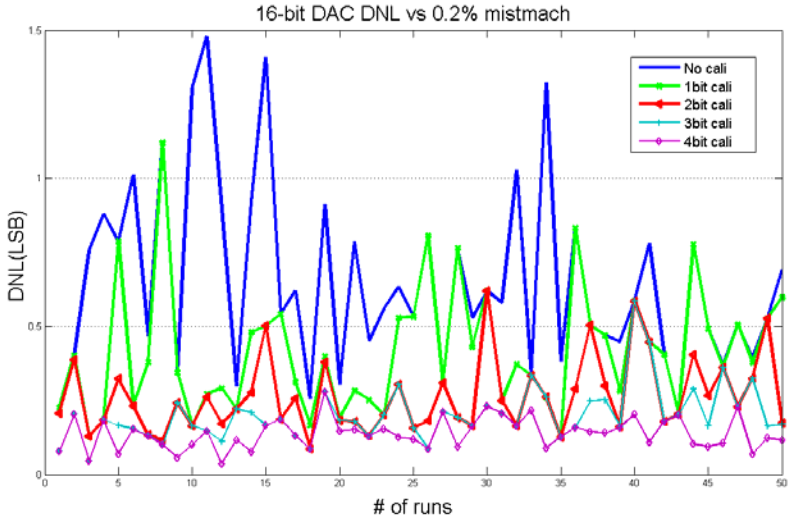

Fig. 7: DNL simulation for different number of calibration bits, for 50 Monte Carlo runs.

The above diagram shows that a 2-bit calibration is sufficient to reach a DNL lower than 0.5 LSB_{rms}.

IV. DESIGN FOR RADIATION HARDNESS AND CRYOGENIC OPERATION

The circuit is radiation tolerant for TID, TIND, SEU and SEL. The design is optimized for cryogenic operation in the range 77-120 Kelvin using proprietary de-rated device models. It operates of course also up to (and beyond) RT, so that it can be placed at different locations in the cryostat allowing the instrument designer to optimize thermal and power management.

Design for radiation hardness was the second key challenge. For the digital part, this project relies on the DARE™ library originating from an ESA/IMEC collaboration. The target process is UMC 0.18µm. This fairly complete library makes the design robust even for extra-terrestrial orbit scientific missions with proven functionality up to 1Mrad TID. Apart from this standard cell radiation hardness, the digital design uses a rad-hard coding style. Hamming codes were introduced to detect and repair faulty states in Finite State Machines and parity checks were implemented for transaction safety. Finally, a watchdog is added to get out of dead lock states if any.

In the analog sections, the radiation hardness is realized by Caeleste's proprietary radiation hard library and design process. Building further on previous experience, this design is expected to be able to withstand far beyond 1Mrad TID and beyond 90MeVcm^2/mg LET for SEL and SEU, even without circuit redundancy. The radiation-hard design has consequences as the design becomes bulkier. However, the analog performances and bandwidths do almost no degrade as the gate areas and parasitic capacitances increase with less than 10%. The area penalty is illustrated in Fig. 8 where a sample logic part in Caeleste's standard library (top) and in Caeleste's radiation hard library (bottom) is place together.

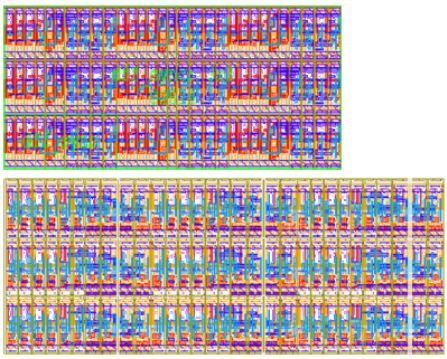

Fig. 8: An array of 3x3 DFF in standard library (top) and in radiation hard layout (bottom)

The challenge of designing for a temperature range of 77K to room temperature was solved defensively. The policy for digital design was to de-rate the library to handle potential set-up and hold time violations as the circuit becomes faster with decreasing temperature. For the analog parts, in the absence of accurate models, the room temperature models were used and de-rated taking into consideration the author's experience and cryogenic characterizations performed on a similar technology nodes. E.g. with decreasing temperature, MOSFET threshold voltage increases as well as mobility. Passive components are carefully selected as some devices will suffer freeze-out, such as lowly doped resistors [5].

V.TESTING

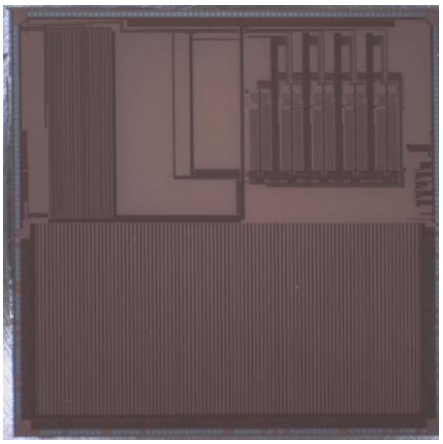

Fig. 9 Die photograph of the ASIC

A. Test system

The chip was processed in UMC's 0.18um technology. The die is shown in Fig. 9. It has a size of 10mm by 10mm.

In order to easily perform the test for both room and cryogenic temperature, two chip-on-board (COB) PCBs were designed for room and cryogenic temperature, both having the same connector to link to the main test board (Fig. 10).

The main test board provides all the analog signals and the power supplies, biasing points and the reference signals. A third board is connected on the other side of the main test board, which will proved all the digital controls, data processing and interfacing the PC via Ethernet .

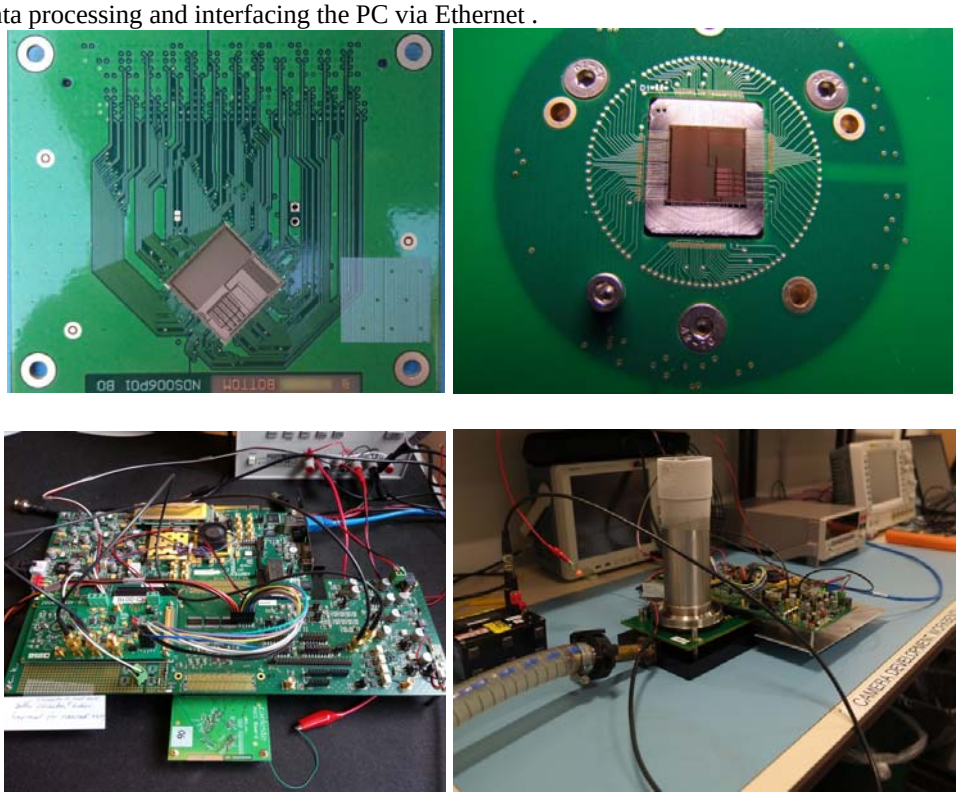

Fig. 10: COB for room (upper-left) and cryogenic (upper-right) temperature test, and the test setups (bottom)

B. Test results

The ASIC is fully functional at 77K and 300K. Some of the analog building blocks do not reach completely the expected performance. New simulations on the ADC showed that certain parasitic capacitances had been underestimated, causing degradation in terms of code gaps. Such insight allows us to reach the specs in the next iteration. Some key specification will be briefly introduced below and summarized in table I.

For the entire ASIC, which is supplied by a single unregulated 3.5V voltage, in nominal conditions, the total current consumption is 55mA at 300K and 60.5mA at 77K where 15% goes to the analog section, 47% goes to the digital processor core, and the remaining 38% is consumed by the digital IOs.

For the supply section, the LDO outputs can be tuned between 1.3 and 3.4V. The PSRR reaches 40dB, the output impedance is smaller 1Ohm regardless the operating temperature.

The 10-bit DACs in the analog section achieve a DNL of 0.07LSB and INL of 0.69LSB, as shown in Fig. 11.

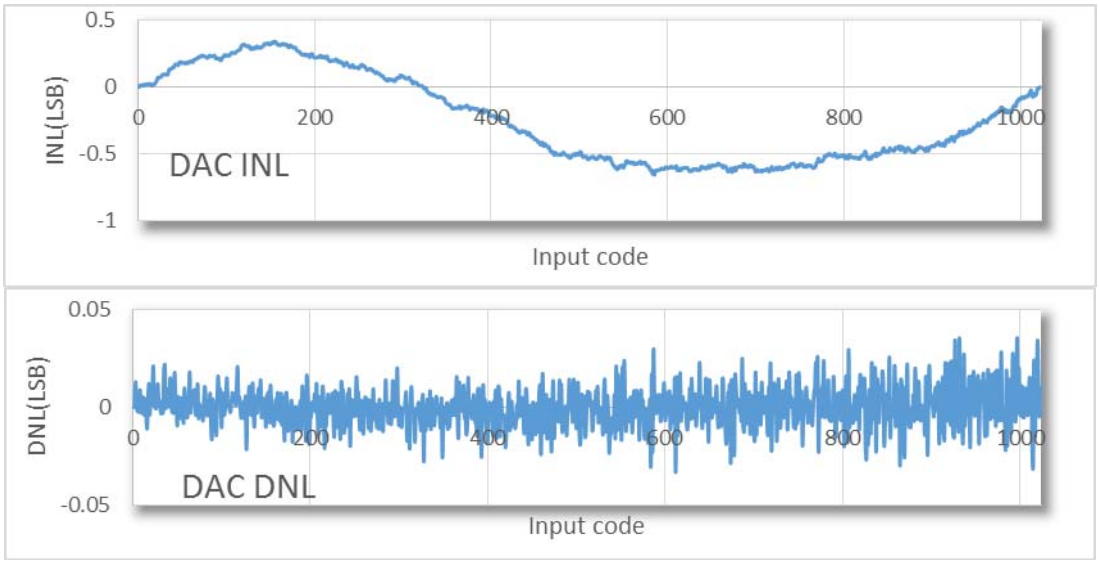

Fig. 11: INL and DNL measurement result of the 10-bit reference/bias DAC

The analog ADC channel can convert the 0-3.3V rail-to-rail input, with 5 different gain settings from 1 to 16 and 8-bit on chip offset cancellation. The 16-bit ADC barely achieves 11-bit linearity at both temperatures. A fixed pattern is visible in conversion curve. The reason was later found and confirmed by re-simulation, essentially an unsuspected crosstalk between a digital bit and the comparator input node. In slower operation and changing the bias conditions of the comparator, the ADC can achieve 12-bit linearity at half the sampling rate (50KHz).

The on-chip switched-capacitor current source for the resistance measurement can offer an accurate current reference of 10.7uA/MHz, and this reference current varies less than 1% over the 200 degree operating range.

Table 1 ASIC performance summary

Specs	Measurement result @ room T	@ cryogenic
Total current consumption	53mA	60.5mA
Regulator PSRR	>40dB	
Regulator Max I output	40mA	
DAC INL	0.7LSB	1LSB
DAC DNL	0.06LSB	0.04LSB
ADC noise	2.5LSB	2.1LSB
ADC fs	100kHz	
ADC INL	78LSB (15LSB@50KHz)	
ADC DNL	76LSB (16LSB@50KHz)	
Current reference	10.7uA/MHz	

VI. CONCLUSION AND FUTURE WORK

The prototype ASIC dedicated to infrared ROIC interfacing, provide the community with a versatile, easy to use, single-chip processing chain for earth- and space borne applications. This prototype ASIC is Silicon proven, with complete functionality at both in room and cryogenic temperature, and all analog block working as specified, except the ADC which has now understood analog performance degradations. It gives confidence for the development of the full-scale ASIC with 32 complete analog channels. Improved calibration and matching concepts will allows us to reduce the footprint and increase the sampling speed of the ADCs, while maintaining the 16-bit nominal accuracy. The analog sampling rate now being 100 kHz, a typical value for scientific applications, will increase for in the next generation with e.g. 12MHz with a reduced accuracy. More sequencer memory will be foreseen as well as 64 digital channels towards the image sensors.

Acknowledgements

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